Design and Implementation of Discrete Multitone Modulator for Digital Subscriber Line Using FPGA

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ABSTRACT

This paper presents a design, simulation and implementation of the Discrete Multitone (DMT) modulator for digital subscriber line (DSL) for both complex and real transmission based on Software Defined Radio (SDR) using FPGA. DMT divides the available bandwidth into parallel sub-channels. There are two techniques to transmit data by DMT. Complex transmission and real transmission .Real transmission is preferred for DSL, since it needs single wire but uses twice number of IFFT. The Simulink HDL Coder has been used for converting the MATLAB-Simulink and M-files models to VHDL language. The verification of the generated VHDL code has been done using Altera- ModelSim, while the synthesis reports and board programming files have been obtained using the Quartus II. The FPGA is used as a platform for SDR. The implementation by using Simulink HDL coder shows the feasibility and flexibility in solving the problems of implementation of the main units of DMT for both complex and real transmission. The main units of DMT are serial to parallel converter,MQAM,IFFT,Parallel to serial and cyclic prefix. The experimental results show that there is coincidence between generated real and complex signal and simulated real and complex signal by generated MATLAB (Simulink and M-file) and Simulink HDL Coder.

Keywords: DMT, SDR, FPGA, HDL coder, IFFT, DSL and MQAM.

تصميم وتنفيذ مضمن متعدد النغمات بأستخدام مصفوفة البوابات المنطقية المبرمجة

الخلاصة

الهدف من هذا البحث هو تصميم وتمثيل وتنفيذ التضمين المتقطع متعدد النغمات (DMT) لل (DSL)بأستخدام البرامجيات المعرفة برمجيا (SDR) بأستخدام مصفوفة البوابات المنطقية المبرمجة (FPGA).حيث يعمل ال (DMT) على تقسيم الحزمة الترددية المتوفرة (Bandwidth) الى قنوات فرعية متوازية. هناك تقنيتين في أرسال البيانات وهما الارسال المعقد(Complex transmission) والارسال الحقيقي (real transmission).وألارسال الحقيقي يكون هو المفضل لل (DSL) لأنه يتطلب استخدام (Single Wire) ولكن يحتاج ضعف نقاط الادخال

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لل (IFFT). تم أستخدام المشفر لغة الكيان المادي الكتلي (Simulink HDL coder) لتحويل (MATLAB-Simulink models) الى لغة (VHDL). استخدم (Altera ModelSim) للتحقق من شفرة(VHDL). تقارير التركيب وملفات البرامج تم الحصول عليها بأستخدام برنامج (Quartus II). مصفوفة البوابات المنطقية الواسعة (FPFA)استخدمت حاملة الى البرامجيات المعرفة راديويا" (SDR). بناء (DMT) بواسطة استعمال مشفر لغة الكيان المادي الكتلي (Simulink HDL coder)أثبت ملائمته ومرونته لحل مشاكل بناء وحدات الارسال المعقد والحقيقي . الوحدات ألرئيسية تتضمن : تحويل البيانات المتسلسلة الى بيانات متوازية (S/P), خارطة الترميز (symbol mapping), محول فورير السريع العكسي(IFFT), تحويل البيانات المتوازيه الى متسلسلة (P/S) والبادئة الدائرية (CP). اظهرت النتائج المختبرية تطابق بين توليد الاشارة الحقيقية والمعقدة عمليا مع اشارات المحاكاة من خلال برنامجMATLAB (M-file) و(Simulink HDL coder)

INTRODUCTION

The increasing users' demand for high bandwidth applications encourages the development and the deployment of new broadband access technologies [1]. The world of information and communication technology (ICT) has changed dramatically, evolving from a means by which information can quickly travel from point to point into an enabling platform for countless new and expanded personal, social, business, and political uses [2].

The industry and the academic world mobilized during the 1980's and the 1990's; develop the digital subscriber line (DSL) technology [3], where the twisted –pair local loop which capable of handling bandwidth up to 1.1 MHz, but the filter installed at the end of the line by the telephone company limits the bandwidth to 4 KHz sufficient for voice communication. If the filter is removed, however, the entire 1.1MHz is available for data and voice communications [4].

The main part in the DSL system is Discrete Multitone Technique (DMT) which is used to convert the narrow bandwidth to broad bandwidth by using a combination of Quadrature Amplitude Modulation (QAM) with Frequency Division Multiplexing (FDM) [4]. However, Orthogonal Frequency Division Multiplexing (OFDM) is used as a technique instead of FDM.OFDM is one of the multi-carrier modulation (MCM) techniques that transmit signals through multiple carriers. These frequencies called (subcarriers).OFDM systems have efficient use of spectrum, resistant to frequency selective fading, Eliminates Inter-Symbol Interference (ISI) and computationally efficient [5]. OFDM main limitation is high synchronism accuracy and large peak-to-mean power ratio due to the superposition of all subcarrier signals [5]. OFDM technique is used for both wired and wireless communications[6]. FFT/IFFT is used to implement OFDM as an efficient technique, which eliminates the redundant calculation which is needed in computing Discrete Fourier transform (DFT) and is thus very suitable for efficient hardware implementation. [7, 8].

The advancements in very large-scale integrated circuits (VLSI) technologies and Software Defined Radio (SDR) provides solution to implement a `flexible OFDM system. SDR can greatly simplify the design of the system since hardware components are replaced by software. SDR offers potentially longer product life, since the radio can be upgraded efficiently, where efficiency can be measured by the cost and the physical volume consumed per information bit [9].

General Purpose Processors (GPPs), Digital Signal Processors (DSPs), Application-Specific Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs) are used as platforms for SDR implemented [10].

There are many methods which can be used to implement SDR in FPGA. The first method writes direct VHDL. The second method includes the schematic. However in 2006, Math Works introduced Simulink HDL Coder, which automatically generates synthesizable Hardware Description Languish HDL Codes. Simulink HDL Coder with MATLAB facility can be considered as a compact package which includes the analysis, design, implementation and verification of DSL [11].

DMT DESIGN PROCEDURE

The proposed design for the DMT Modulator for DSL is shown in figure (1). Table (1) shows the proposed design parameters of the system. The main parts of the proposed:

- Serial to Parallel (S/P): The serial data stream is mapped to symbols with a symbol rate of 1/Ts. For modulation scheme 8QAM, the (S/P) transmits 3 bits for each sub channel for the next block
- QAM modulator: Each symbol is mapped to a complex symbol stream using, the MQAM modulation.
- IFFT: An inverse FFT is computed for each set of symbols, delivering a set of complex samples for complex transmission. And real samples by using 2N IFFT for real transmission.

To transmit N distinct subcarriers (with frequency integer multiples of f_s) using only the real signal, the sampling frequency should be $2N \cdot f_s$, to allow the recovery of N distinct sub-channels and the imaginary part should have a constant value, independent of the modulated data, that would be known at reception and would not be transmitted; this leads to the transmission of a single real signal(the implementation of DMT demodulator is out scope of the works).In order to fulfill the above requirements, two conditions should be satisfied are:

1. The modulator implemented with an IFFT block will have 2N inputs, instead of N;
2. The QAM modulating levels of the tones with index N+1, ..., 2N-1, will be the complex conjugates of the levels transmitted on the tones with 1,2,…...N-1

The above two conditions can be expressed as follows:

The complex modulating symbols on the tones [12, 13]

$$X_k = a_k + jb_k \quad .. \quad k = 1,2,\dots,N-1 \qquad \dots(1)$$

$$X_{2N-k} = (X_k)^* = a_k - jb_k \quad \dots k= N+1 \dots 2N-1 \qquad \dots(2)$$

where : a_k = real value, b_k = imaginary value

The output of the IFFT is:

$$x(n) = 2\sum_{k=1}^{N-1}\left[a_k \mathrm{Cos}\left(\frac{2\pi kn}{2N}\right) - b_k \mathrm{Sin}\left(\frac{2\pi kn}{2N}\right)\right], n = 0, \dots 2N-1 \dots (3)$$

- Cyclic prefix: The Cyclic Prefix (CP) is a copy of the last N samples from the IFFT, which are placed at the beginning of the DMT frame to overcome ISI problem. It is important to choose the minimum necessary CP to maximize the efficiency of the system [12].

Figure (2) describes the design and implementation procedure used for the typical SDR system

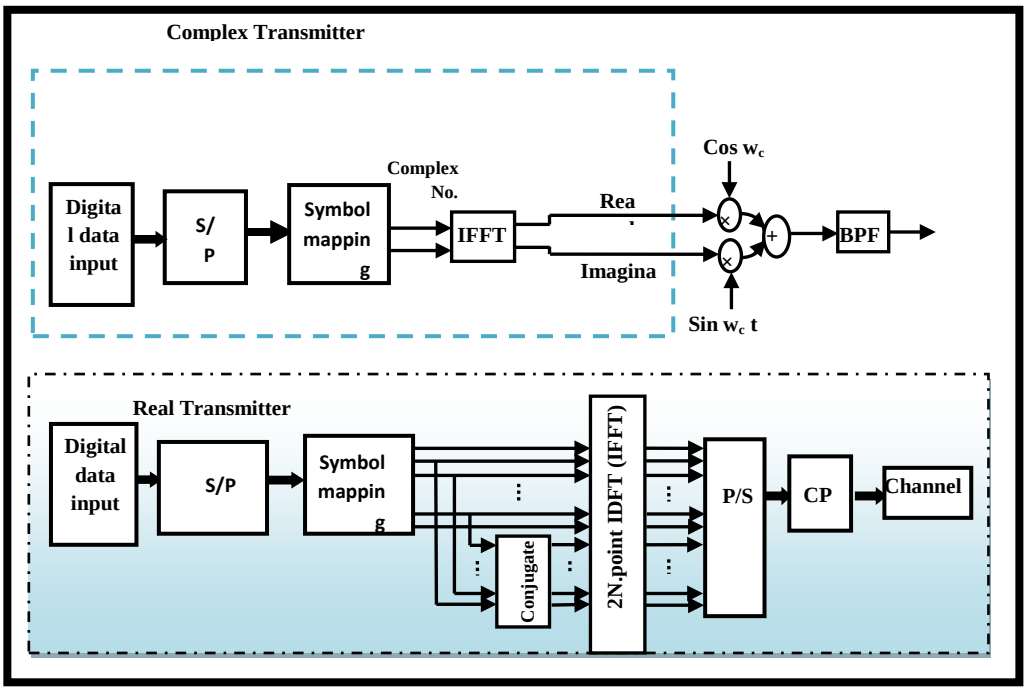


Figure (1) Block diagram of the proposed system [12].

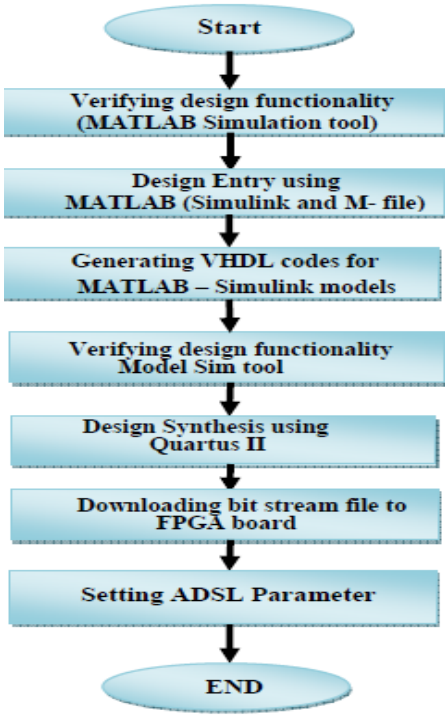


Figure (2) Design procedure of the typical SDR System

Table (1) Design parameters goals.

Parameter	Selected types of complex system	Selected types for real system
Modulation type	256QAM	128QAM
Number of sub channel	256	128
IFFF size	256points	256 points
Cyclic Prefix Length	32 samples	32 samples
Data rate	1.104 Mbit/Sec.	1.104 Mbit/Sec.
Sampling Frequency	2.208 MHz	2.208 MHz
Subchannel B.W	4.3125 KHz	8.625 KHz

SIMULATION RESULT BASED ON MATLAB

GENERATION OF SIGNALS FOR ADSL USING 256 IFFT FOR COMPLEX TRANSMISSION

Figure (3) shows the input signal for serial to parallel converter and its output signals for 256 QAM. Figure (4) shows the output signal for 256QAM. Figure (5) shows the spectrum of the output signal for 256 IFFT signal.

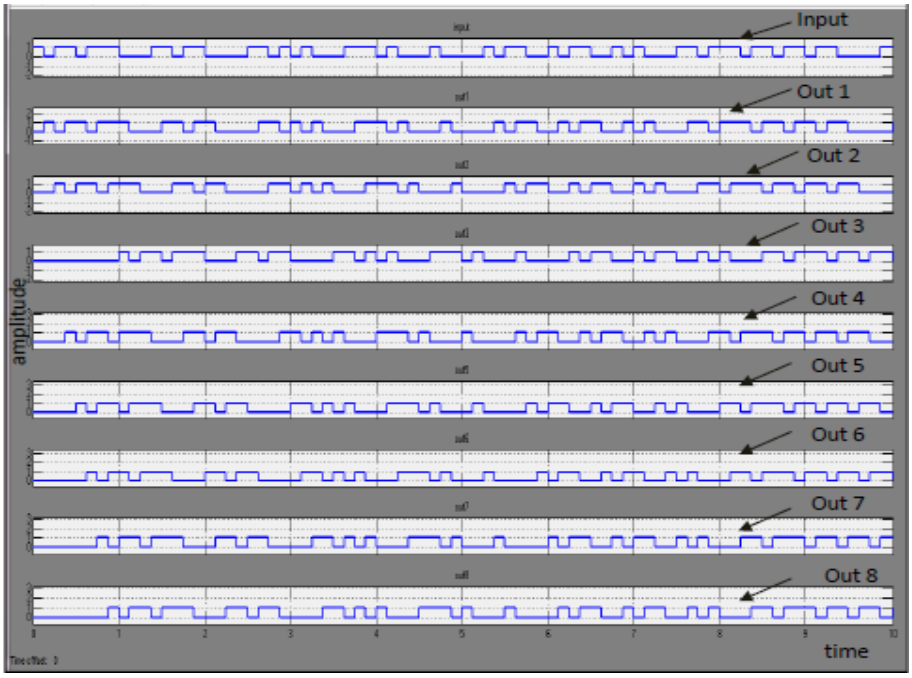


Figure (3) Input and output data from serial to parallel converter for complex transmission

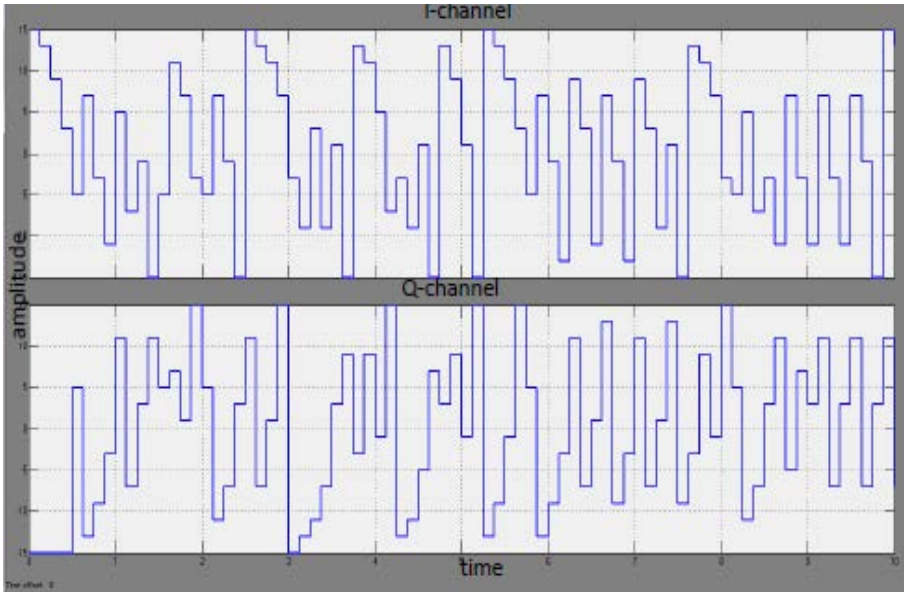


Figure (4) Output signal for 256 QAM for complex transmission

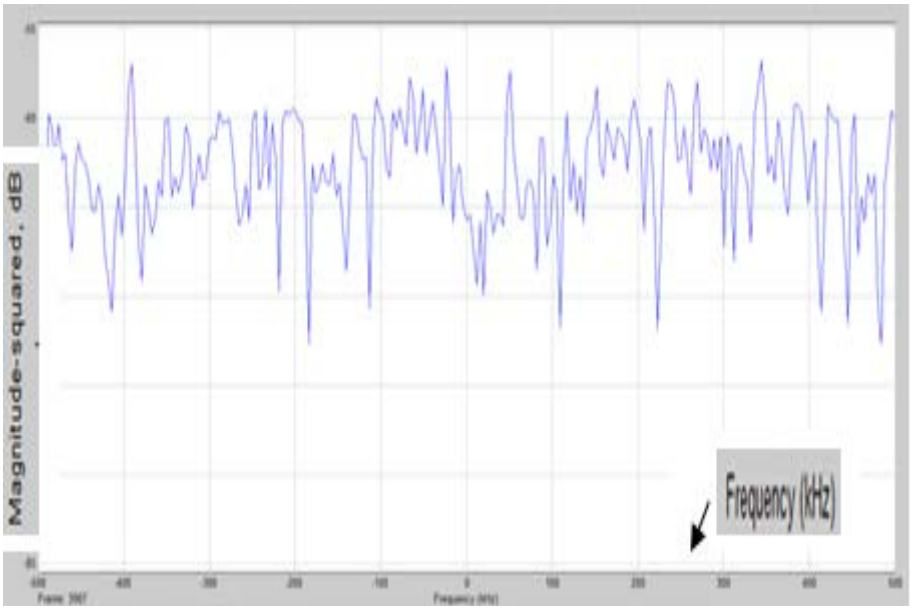


Figure (5) Spectrum signal for 256 IFFT (for giving input data for complex transmission)

GENERATION OF SIGNALS FOR ADSL USING 256 IFFT FOR REAL TRANSMISSION

Figure (6) shows the input and output signal for serial to parallel converter. Figure (7) shows the output signal for 128 QAM (for real transmission twice the size of QAM elements are being used, the input signal and their conjugate). Figure

(8) the output signal for 256 IFFT. Figure (9) shows the spectrum signal for 256 IFFT. Figure (10) shows the output signal after a cyclic prefix for 256 IFFT.

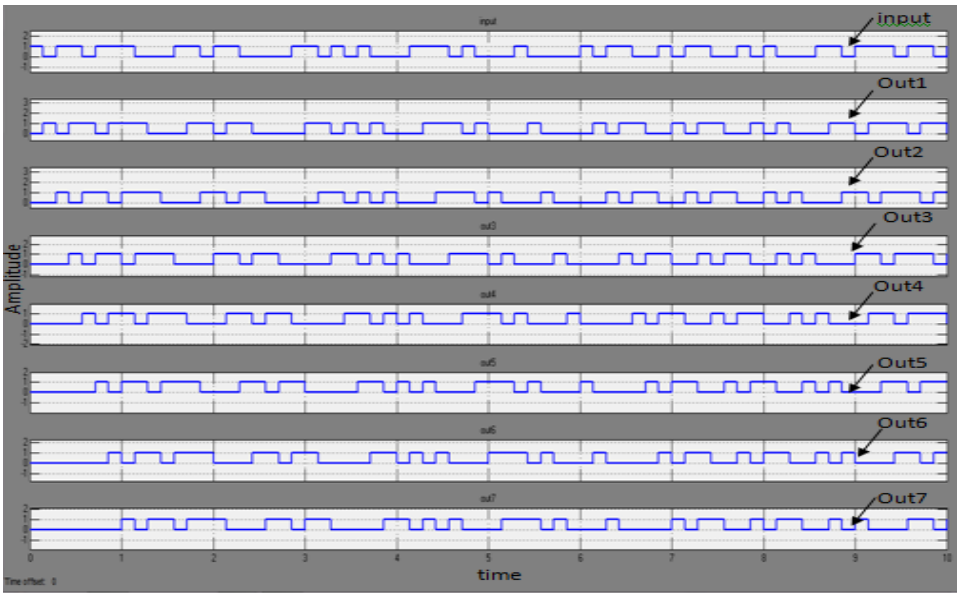


Figure (6) Input and output data from serial to parallel converter for128 QAM for real transmissions.

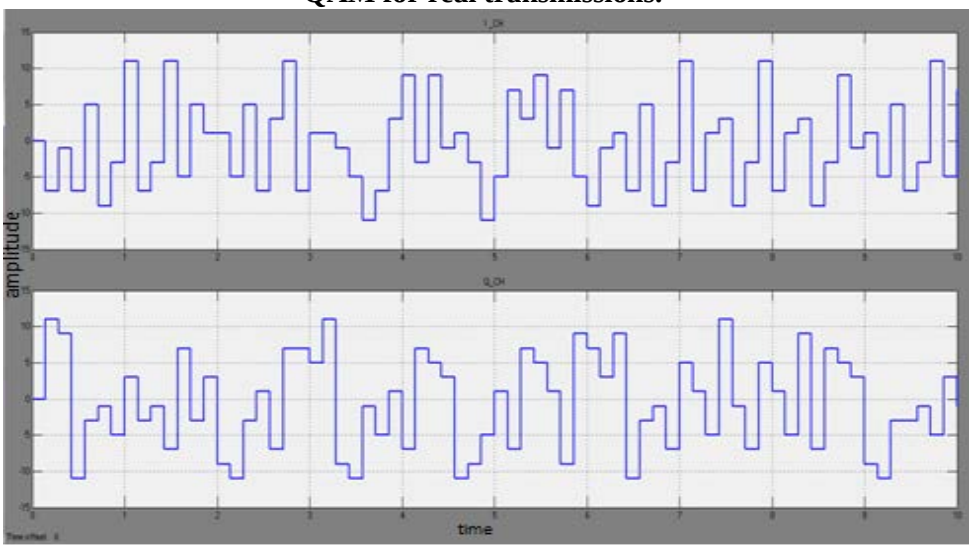


Figure (7) The output signal for 128QAM.

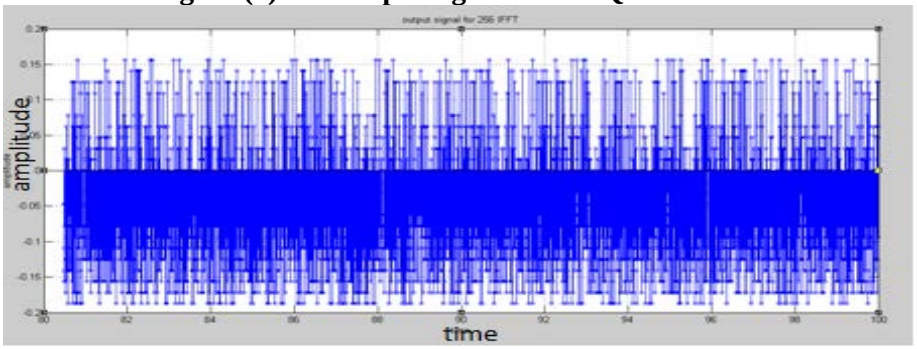


Figure (8) The output signal for 256 IFFT for real transmission

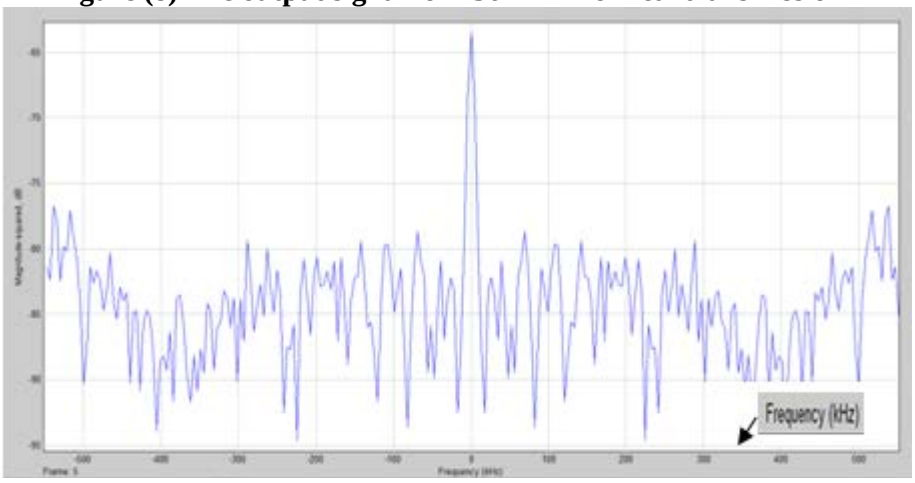


Figure (9) Spectrum signal for 256 IFFT for real transmissions.

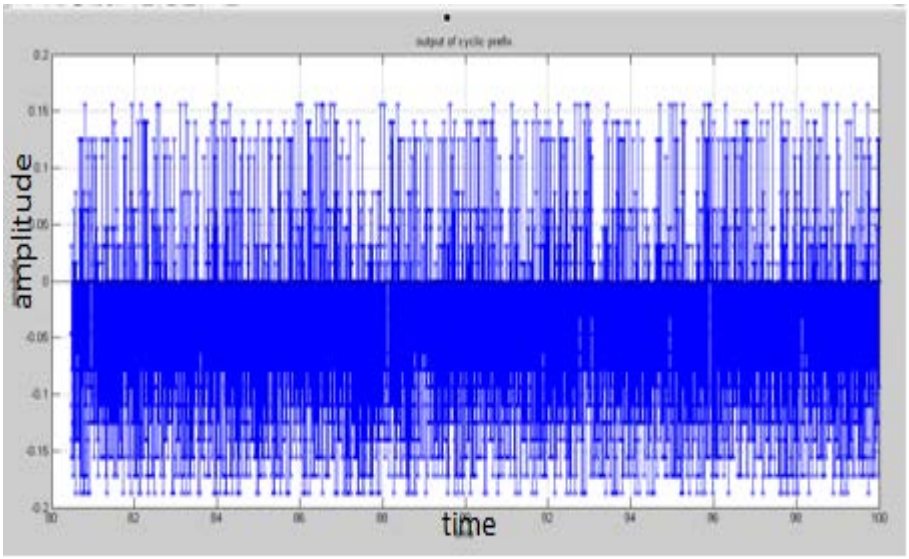


Figure (10) The output signal after cyclic prefix for 256IFFT for real transmission

SIMULATION RESULTS BASED ON MODELSIM

SIMULATION RESULTS BASED ON MODELSIM FOR DMT MODULATOR (256IFFT) FOR COMPLEX TRANSMISSIONS.

The simulation results obtained by using ModelSim-Altera 6.5a (Quartus II 9.1) represent the second step in the simulation process. Figure (11) shows the input signal for serial to parallel converter and its output signals for DMT modulator (256IFFT). Figure (12) shows the output signal for 256 QAM for DMT modulator. Figure (13) shows the output signal for 256 IFFT for DMT modulator. Figure (14) shows the output signal after cyclic prefix for 256 IFFT for DMT modulator.

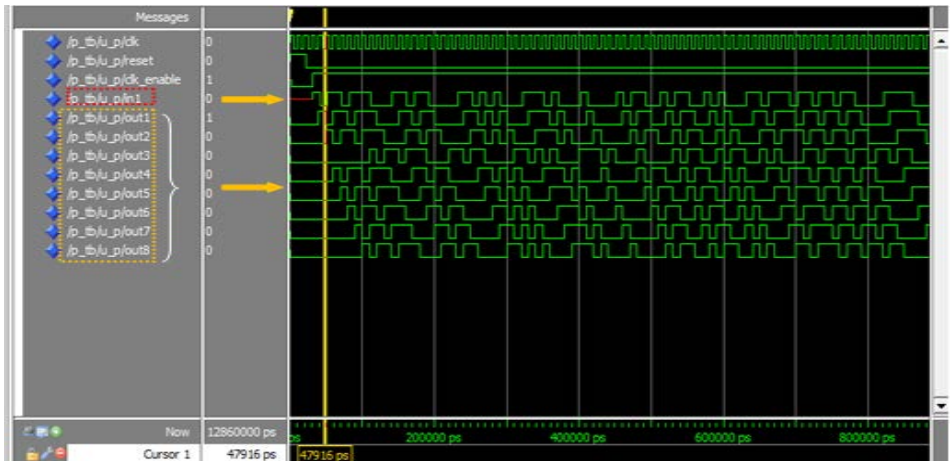


Figure (11) Input and output data from serial to parallel converter (256IFFT) for complex transmissions

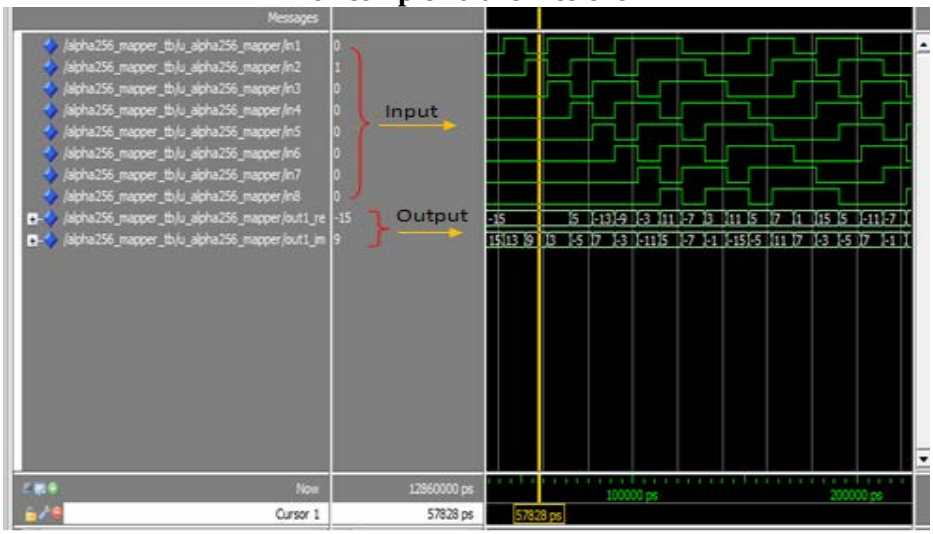


Figure (12) The output signal for 256QAM for complex transmissions.

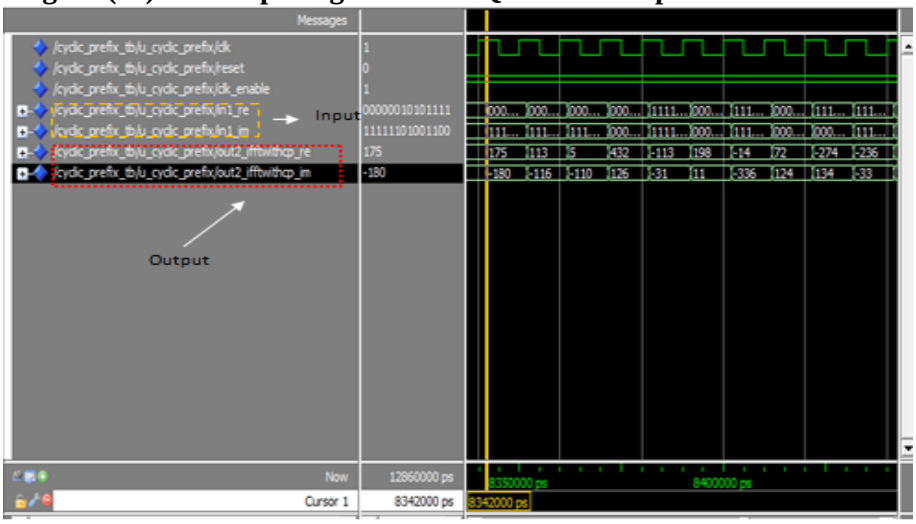


Figure (13) The output signal for 256 IFFT for complex transmissions

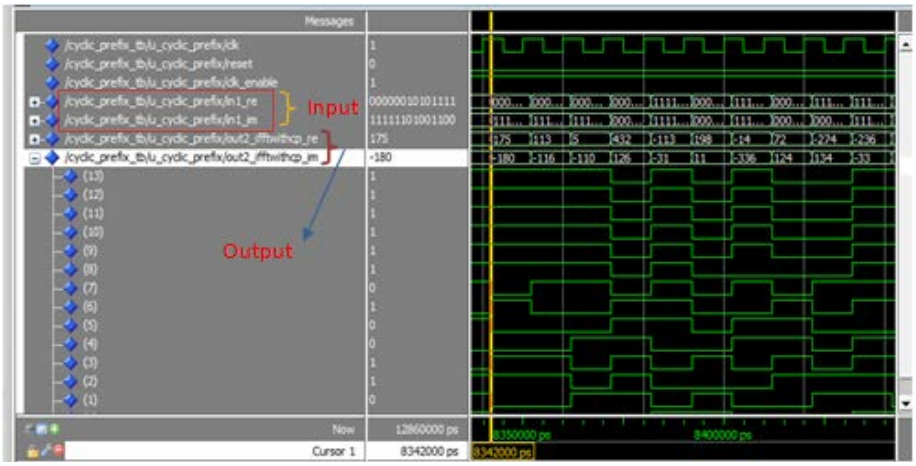


Figure (14) The output signal after cyclic prefix (for 256IFFT)

SIMULATION RESULTS BASED ON MODELSIM FOR DMT MODULATOR (256 IFFT) FOR REAL TRANSMISSIONS.

Figure (15, 16, 17, and 18) show the input and output data for (S/P) converter for 256 IFFT, the output signal for 128 QAM, the output signal for 256 IFFT and the output signal for (P/S) converter.

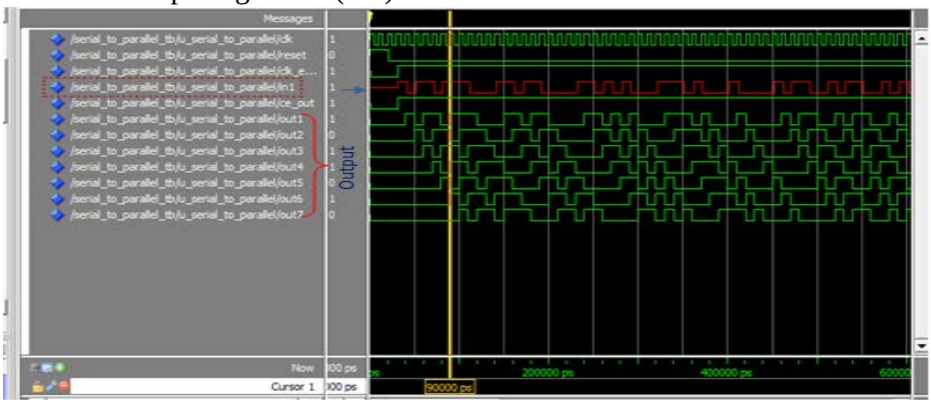


Figure (15) Input and output data from serial to parallel converter for (256IFFT) converter for real transmission.

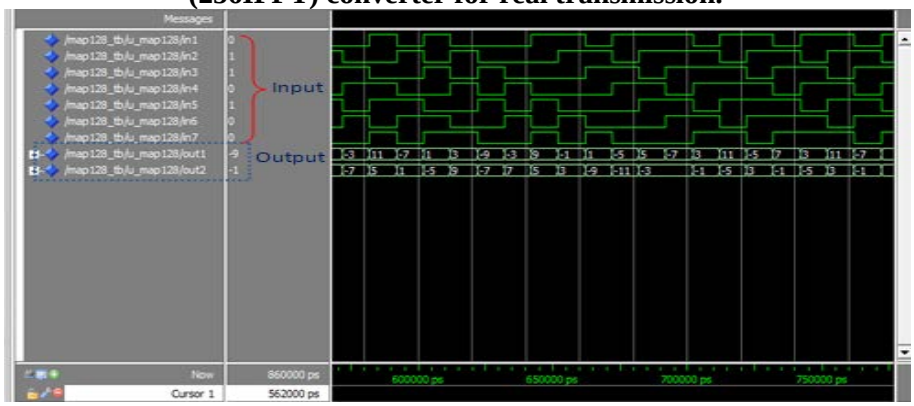


Figure (16) The output signal for 128 QAM for real transmission.

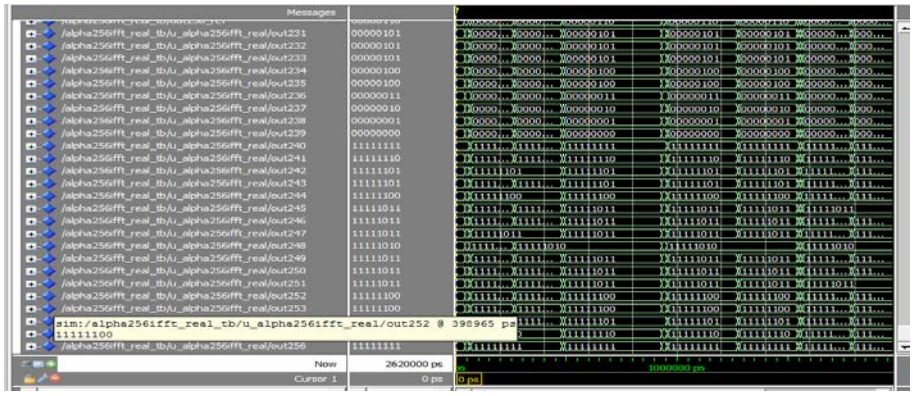


Figure (17) The output signal for 256 IFFT for real transmission

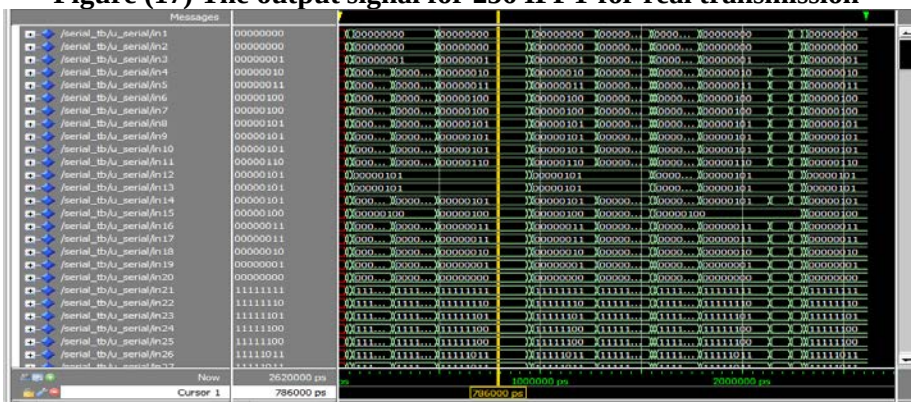
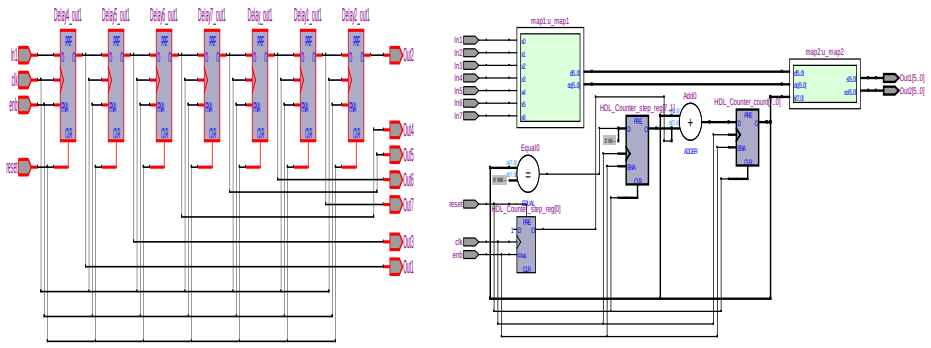


Figure (18) The output signal from parallel to serial converter for (256IFFT) for real transmission.

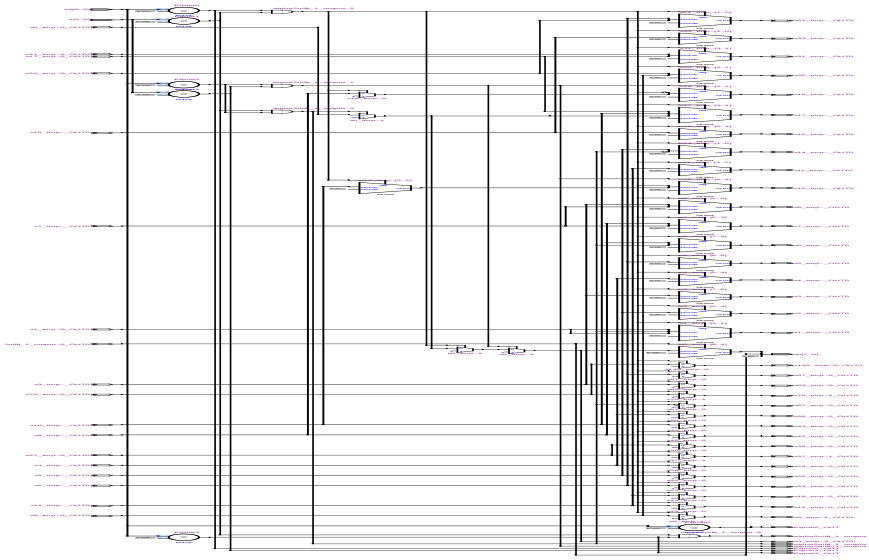
SYNTHESIS OF THE DMT MODULATOR FOR REAL TRANSMISSION BASED ON FPGA

Figure (19) shows the Register Transfer Level (RTL) implementation of SDR system for DMT modulator (256 IFFT) for real transmission.

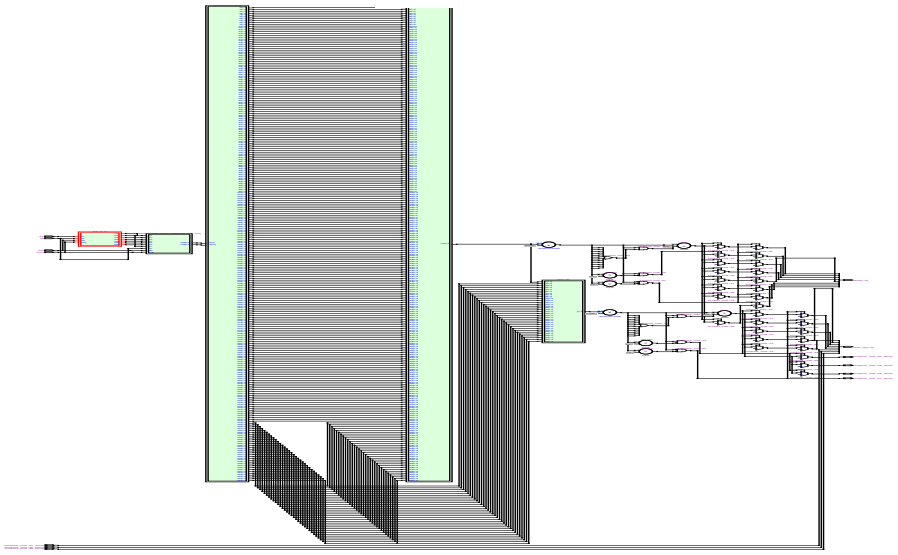


(a) **(b)**

Figure (19) To be Continued.



(c)



(d)

Figure (19) The RTL implementation (a) Serial to Parallel(S/P) converter (b) 128 QAM (c) 256 IFFT. (d) DMT modulator for (256 IFFT)

EXPERIMENTAL RESULT

DAC is used to convert output digital data from FPGA to an analog signal in order to represent the output signal as shown in figure experiment. There is coincident between the output signal and the expected output signal for a given the input signal. Figure (20) shows the practical connection of to DMT modulator. Figure (21-a) shows the input signal from the signal generator to DMT modulator for real transmissions .Figure (21-b) shows the output signal of (256IFFT) for real transmission.

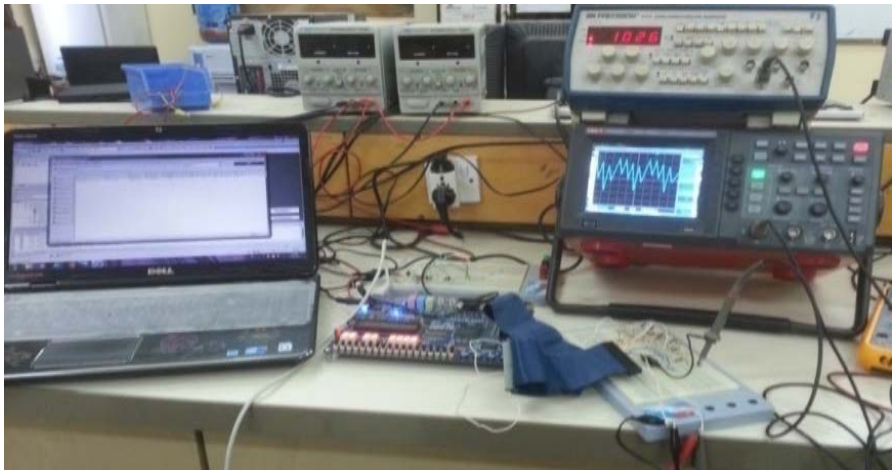


Figure (20) Practical connection of DMT modulator for real transmissions

(a) **(b)**

Figure (21) a- The input signal to DMT modulator for real transmissions.
b- The output signal for (256IFFT) for real transmissions

CONCLUSION

- FPGA offers flexible solutions for DMT implementation because it provides high speed, high level of integration; low development costs and needs low power.
- Simulink HDL Coder proves the capabilities to generate Hardware Description Language (HDL) code to MATLAB model (Simulink and M-file) for main units of DMT. The following main units which are designed, implemented and verified:-
  - Serial to parallel converter
  - Symbol mapping (baseband modulators) to convert the input data to the (complex levels) compatible with the QAM modulators of the DMT.
  - Inverse Fast Fourier Transform for real and complex transmission
- The real transmission needs twice the number of points of IFFT to increase the complexity of the system but used a single wire instead of two wires.
- The simulation results of the MATLAB and ModelSim show the coincidence between the results

- Experimental results of the DMT approximately coincide with simulation results which are obtained from MATLAB and ModelSim results with small distortion.

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