Design and Implementation of Programmable Multi-Mode Digital Modulator for SDR Using FPGA

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Accepted on:22/10/2013 & Received on:6/2/2014

ABSTRACT

The design of programmable multi-mode digital modulator for software defined radio (SDR) technology using FPGA is developed and investigated in this paper. The system generator from Xilinx and MATLAB tools are used for FPGA design as well as the implementation of the modulator over a Virtex-4 FPGA board. The HDL language on Xilinx ISE is used to generate the bit stream of the modulator algorithms into ADC/DAC device and FPGA board. The modulated signal obtained from MATLAB simulation is evaluated with the tested signal to verify the system functionality. Lastly, the optimally synthesized netlist of the integrated design is downloaded into Xilinx Virtex-4 FPGA MB development board. The verification of DAC output signal via oscilloscope demonstrate the empirical real-time signals similar to the simulated waveforms. Results shows the successfully implementation steps as timing constraint of FPGA is accepted without error. The proposed design is promising to enhance the current and next generation of communication systems with less power consumption compared with conventional design in term of FPGA Slices and Look Up Tables (LUTs) during the implementation process. The improvement in Slices and LUTs produce by ISE project utilization summary is 65% and 79% respectively.

Keywords: Programmable Digital Modulator, SDR, FPGA, MATLAB, System Generator

تصميم وتنفيذ مضمن رقمي مبرمج متعدد الاغراض باستخدام بورد مصفوفة البوابات البرمجية

الخلاصة

هذا البحث يقدم تصميم معدل رقمي مبرمج متعدد الاغراض باستخدام بورد مصفوفة البوابات البرمجية والذي تم تطويره والتحقق منه. استخدم في هذا البحث برنامج ماتلاب ومولد النظام لتنفيذ المعدل في البورد المبرمج. تم توليد لغة وصف البورد باستخدام البرنامج التكاملي ومن ثم توليد جداول لوغارتم المعدل الى البورد المبرمج. الاشارة المعدلة بالمحاكات تم مقارنتها بالاشارة الحقيقية وتم تقييمها باستخدام مولد النظام. تم مقارنة نتائج المحاكات مع نتئج التنفيذ واثبتت تطابقهما. بينت النتائج تنفيذ المشروع بنجاح كافة الخطوات كون المحددات الزمنية للبورد قبلت بدون اخطاء. التصميم المقترح يعزز انظمة الاتصالات الحالية والمستقبلية باقل قدرة مستهلكة بالمقارنة مع التصاميم الحالية محسوبة من خلال كمية الشرائح والجداول المستخدمة في مصفوفة البوابات المبرمجة عند التنفيذ. التحسن

https://doi.org/10.30684/etj.32.7A.4
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بعدد الشرائح والجداول بحدود 65% و79% على التوالي حسب ما جاء بملخص المشروع المتولد من البرنامج ISE.

INTRODUCTION

The current and future wireless communication standards are rapidly changing and growing along with conventional standards. The conventional mobile phone could support only limit number of standards and the modern technology has changed toward the software defined radio (SDR) idea [1]. The technology of SDR need reconfigure digital components to performs the necessary digital signal processing (DSP) with transceiver of baseband information in the intermediate frequency (IF). [2]. The requirements of mobile handset nowadays is essentially support the implementation of physical layer protocols of many communication mode to provide the user demand at anytime and anywhere within single device [3]. The DSP and FPGA are able with signal processing functionality for hardware realization of the communication standards[4]. The SDR facilitate the users and industrial to improve their products in order to achieve the user demands [5]. Numerous techniques have evolved to design programmable radio of SDR. The concept of parameterization and dynamic reconfiguration in the digital radio system design which can integrate 2G and 3G standards in ordinary stage was earlier introduce by J. Motila at 1991. Several silicon solutions for design the SDR by the most excellent possible hardware selections has been fined out in [6]. Low power SDR prototype module and suitable for many mobile air interface was developed by[7]. A real time SDR test bed for baseband processor of wireless standards implementation on general purpose processor (GPP) is described in [8]. A low cost design has been adopted for baseband processing in SDR design proposed by [9]. A new design framework for common baseband processing after exploring the algorithms for 3G and 4G systems has been produced by [10]. One of the more important binary modulation techniques which has used only two phases of the carrier at the same frequency is the binary phase shift keying (BPSK) and quadrature amplitude modulation (QAM) [11]. This type of modulation could be generated with bandwidth efficiency and symbol error performance. The latest version of ISE (Integrated Software Environments) from Xilinx [12] could be used to generate the BPSK and QAM bit streams to Virtex-4 FPGAs [13] after the HDL code is built by ModeSim [14] and synthesis tool introduced for Simplicity [15]. The Virtex-4 FPGA board is a development platform based on a Xilinx products[15]. It provides a development kit for embedded applications of digital signal processing (DSP). The web pack ISE software from Xilinx is completely featured front to back FPGA design solution which offers HDL synthesis device fitting and JTAG programming. The BPSK is a simple one dimension modulation scheme which is a phase of carrier sinusoidal signal changes suddenly by 180 or pi radian for every broadcast of modulating binary sequence[16] . The Block diagram of QAM transmitter using FPGA is shown in Figure 1. The input of QAM with one or zero values is mapped to symbol through polar conversion and local oscillator generate carrier sinusoidal signal with specific frequency to be mixed by multiplier to produce QAM modulating signal[17].

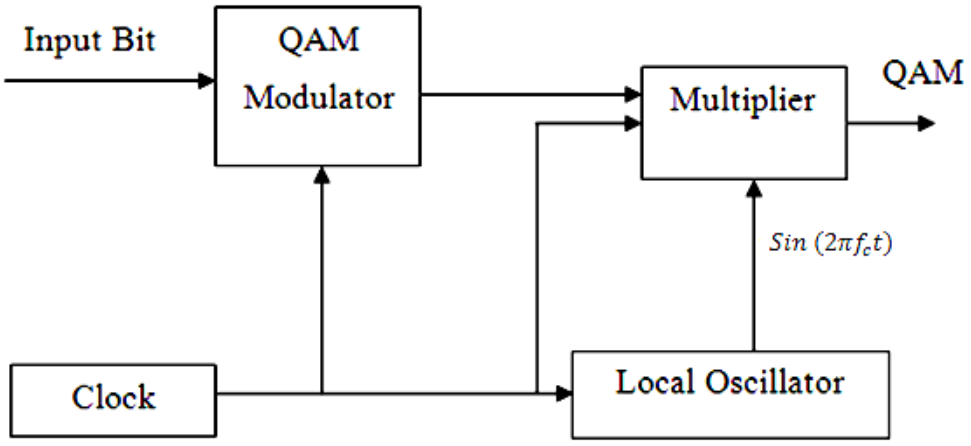


Figure (1) Block Diagram of QAM Modulator

The proposed modulator could be integrated with QAM modulator communication standards and with all standard illustrated in Table (1). The capability of single device to work with multiple wireless communication standards is engaged under SDR technology[18]. The proposed programmable modulator in this paper could performs any scheme of QPSK, BPSK, QAM and any other digital modulator to serve the SDR transceivers.

Table (1) Data rate and modulation schemes of multiple wireless standards

Standard	Data Rate	Modulation Type
Deep Space Telemetry	32300 Mbps	BPSK
DVB	9.14 Mbps	QAM
IS-95	1.2288 Mbps	QPSK
IS-54/IS-136	30 Kbps	DQPSK
GPS	2 Mbps	QPSK
UMTS	3.6864 Mbps	QPSK
DVB	9.14 Mbps	QAM
GSM	1.2 Mbps	QAM/GMSK
Cable Modem	More than 20 Mbps	BPSK

The principle of BPSK modulator, the binary data is converted to binary code format and multiplied by carrier signal (Fc) as illustrated in Figure (2). If m(t) is bipolar format signal, c(t) represent the carrier signal and s(t) is modulated signal then the BPSK signal could be represented as[19]:

$s(t) = A_c Sin\ (2\pi f_c t)$ if m(t) = logic 1 (1)

and

$$s(t) = -A_c Sin\,(2\pi f_c t) \qquad \text{if} \quad \text{m(t) = logic 0} \qquad (2)$$

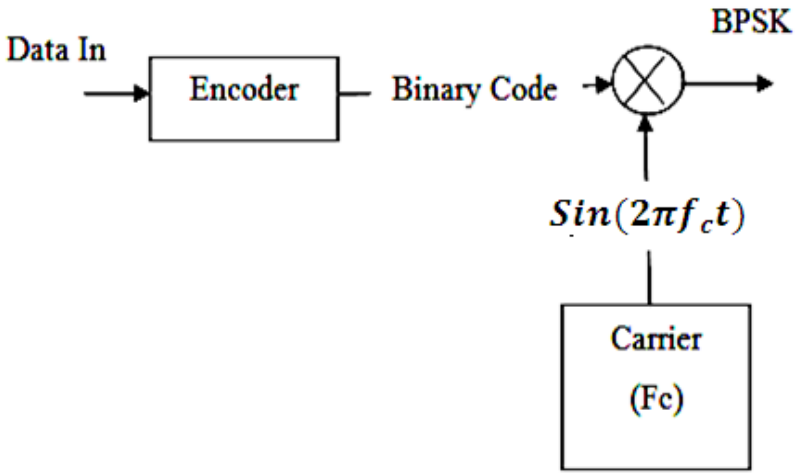


Figure (2): Bock diagram of BPSK modulator design

The bit error rate (BER) is decrease exponentially as SNR increase with AWGN channel which produce good signal quality at the receiver side[20]. Though, the symbol error rate in BPSK is less compared with other modulator techniques as clearly shown in Equation (3). Then, the BER of BPSK could be represented by mean of average energy per bit (E_b) and noise power (N_0) as in [21]

$$P_b = Q\left(\sqrt{\frac{2E_b}{N_0}}\right) \qquad (3)$$

In the case of QAM modulation, the variation of the one used for PSK. Hence, the generalized PSK allows changing both amplitude and phase and all points lie in circle. Therefore, the I and Q values are related to each other. So, all value have the same values. If the amplitude changed from symbol to symbol, then the modulation is called quadrature amplitude modulation (QAM). This techniques could considered as linear combination of two DSB-SC signal. Therefore, its AM and PM modulation as shown in Equation (4).

$$s(t) = \underbrace{\left(\sqrt{\frac{2E_s}{T}}\cos(\theta(t)\cos(2\pi f_c t)\right)}_{\text{I}} - \underbrace{\left(\sqrt{\frac{2E_s}{T}}\sin(\theta(t)\sin(2\pi f_c t)\right)}_{\text{Q}} \qquad (4)$$

To create the hybrid type of modulation that varies both amplitude and phase, Equation (4) could be used as QAM modulator. For example, if we have 16 symbols represented a four bit word, then this modulation called 16 QAM modulator.

Implementation Design Flow

In this section, the developments of configurable baseband QAM modulator is explained in detailed. The proposed flow chart of design and implementation of QAM model could be divided into 2 parts specifically software and hardware, as illustrated in Figure (3). The proposed flow shows the simulation and implementation steps by using MATLAB and Xilinx System Generator's blocks. Following the simulation of QAM model in fixed point and verification with SIMULINK model, the next step is the implementation of the model in the FPGA form. To implement the QAM modulator model in FPGA, Xilinx presents many tools to download the designed model as a bit-stream to FPGA. The ModelSim blocks are an helper block used to design the Verilog module of integrated design. The ModelSim output is feed back to SIMULINK for verification.

The implementation steps are read in the constraints file that consists of three main steps: translate, map, and place & route. The translate step basically compress the output of the synthesis tool into a large single netlist. A netlist in general, is a large list of gates which is compressed at this stage to remove any pecking order. The map step collect the logical symbols in the flattened netlist into physical components, specific to the target device. The place and route step places each of these physical components onto the FPGA chip and connects them through the switch matrix and dedicated routing lines.

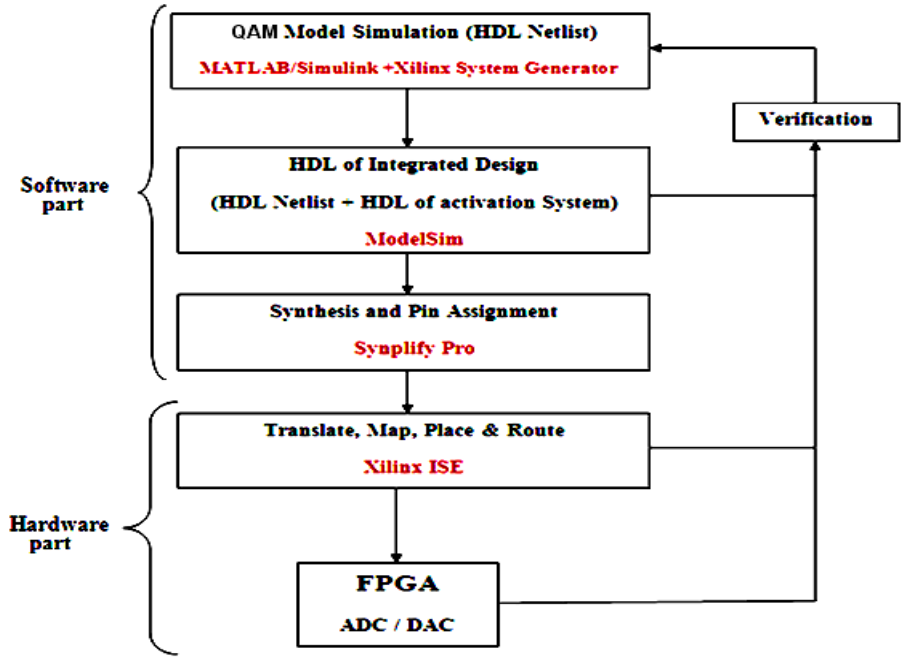
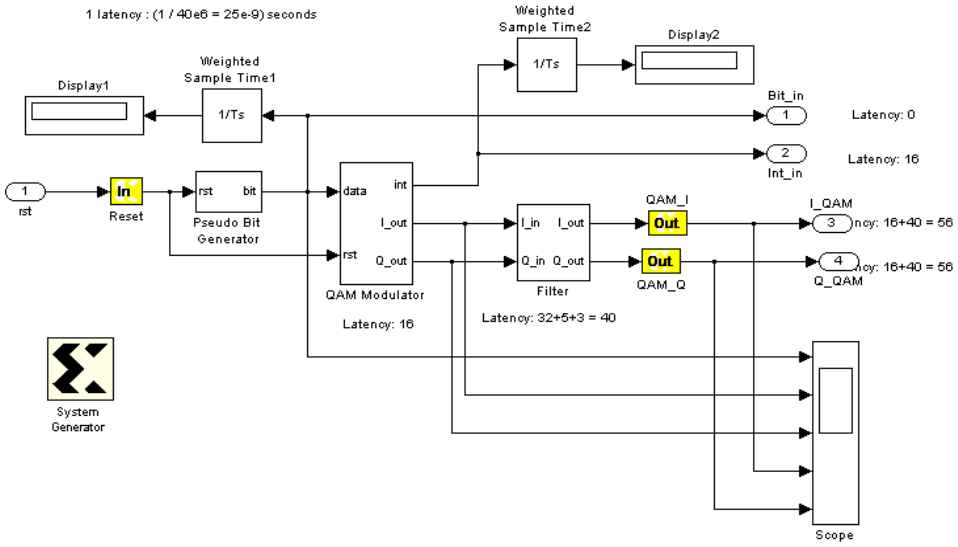


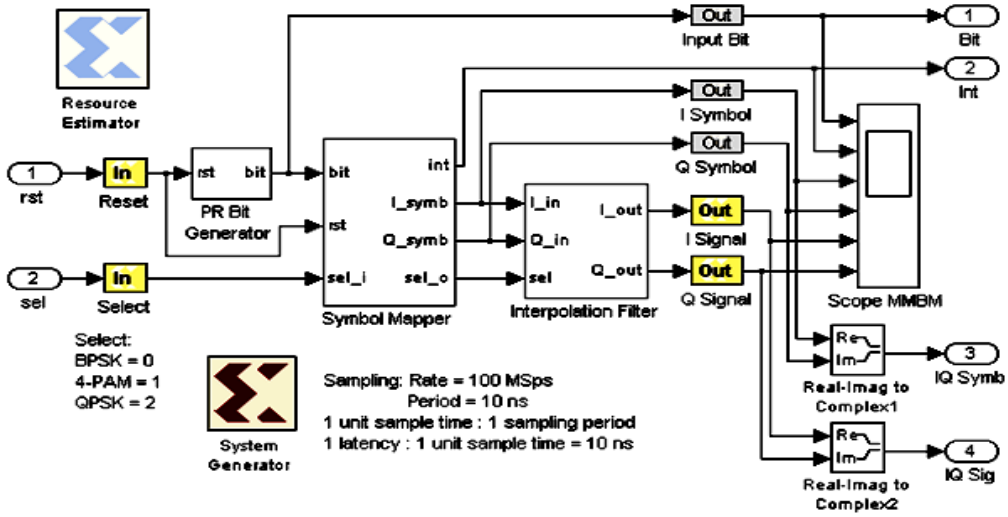
Figure (3): Proposed Simulation and implementation flow

QAM and BPSK Baseband Modulator Design

The DSP model of top level QAM in System Generator/Simulink environment is illustrated in Figure 4. It comprises of main subsystems of PR Bit Generator, Symbol Mapper and Interpolation Filter. The operations of interior subsystems and practical blocks is explained in detailed as below.



(a)QAM Modulator



(b)BPSK Modulator

Figure (4) DSP Model of digital (a)QAM and (b) BPSK Modulator using System Generator.

The System Generator [22] block is required for Simulink model that contains any block from Xilinx block set and is normally located at the top level. It is used to set Simulink system period: 1 unit, FPGA system clock and sample rate f_s = 100 MSps. In addition it is used to generate HDL netlist of QAM with test-bench file written in Verilog codes. Finally, it is convenient to represent the normalized sampling period T_s as 1 unit sample time, or 1 latency. The Resource Estimator block is used to compute an estimation of FPGA resources for implementing the QAM enclosed within Xilinx Gateway.

The input ports of the top level QAM model are Xilinx Gateway in blocks (reset and select) is sampled at T_s of 16 units sample time to form Boolean output to the inputs *rst* of the PR Bit Generator and Symbol Mapper subsystems. The IQ symbols and IQ baseband modulated signals are grouped in pairs by Real-Imag to Complex1 and 2 blocks respectively for better wiring illustration.

The fixed point principles of the inputs are transformed to floating point double precision values by Xilinx Gateway Out blocks to form symbol integer output. The simulation results of top level QAM displayed in the Scope block are illustrated in Figure 5. For noiseless low-pass equivalent channel, the IQ input signals received by the BPSK are identical to the IQ baseband modulated signals.

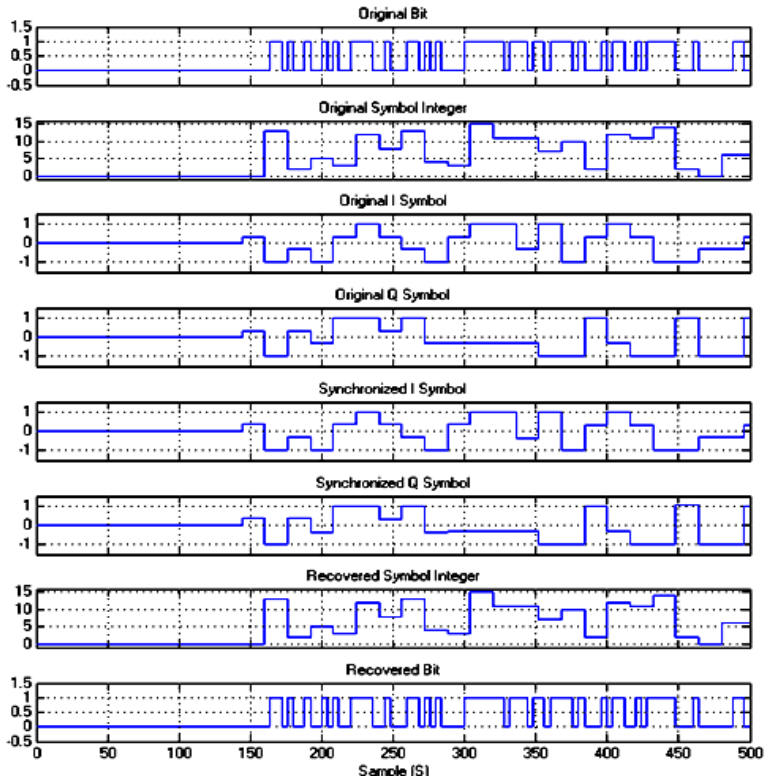


Figure (5): Simulation Results of QAM

After matched-filtering with adjusted gain, the IQ filtered data resemble the IQ baseband modulated signals. Then, the IQ synchronized symbols would be the optimal IQ filtered data samples that have been captured at optimum sampling instant. In order to verify performance of the BPSK system implemented using FPGA via DAC in P240 Analog Module, the sharp-edged recovered bits were intentionally pulse-shaped to become the smoothed bits. However, it can be found that the recovered bits and smoothed bits for QAM are all equivalent.

HDL Design

The configurations of ADC and DAC are set during Serial Programming Interface (SPI). The Verilog HDL module of setup configuration and Verilog HDL netlist of QAM modulator are verified firstly before combining both to become HDL module of integrated design. Both the simulation results in ModelSim environment are shown in Figure 6. Considering the real-time implementation of integrated design of QAM transmitter and setup configuration using FPGA and P240 Analog Module, the ADC and DAC in P240 should be configured first prior to the running of DSP design, in order to avoid instability of ADC and DAC that can produce undesired outputs to or from FPGA during process of configuring ADC and DAC. Consequently, the clock enable (ce) of FPGA design is disabled during the transfer of SPI codes to ADC and DAC in P240. Controlling the main *ce* would be easier rather than clock enable clear (*ce_clr*) which requires additional logics to adjust sampling phase of all the multi-sample data when it is asserted.

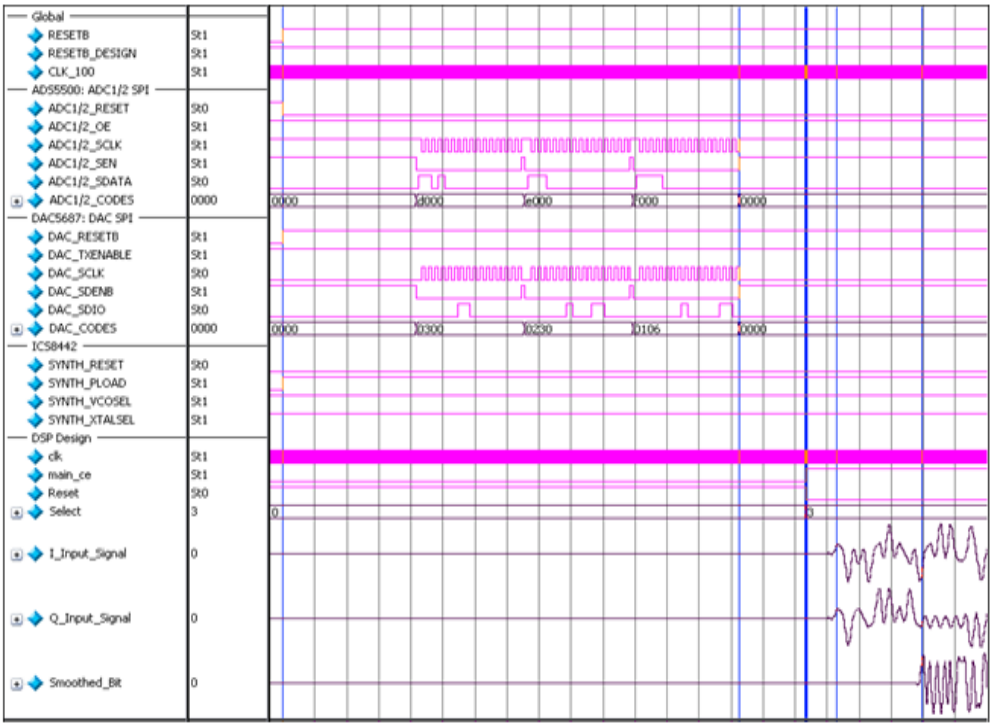


Figure (6): HDL simulation result of QAM Netlist

Though, the Xilinx ISE group has its own synthesis tool "Xilinx Synthesis Technology" (XST), but it can only synthesize HDL netlist generated from System Generator. Consequently, Synplify Pro software is used to execute logic synthesis for the HDL module of integrated design in 2 stages of logic compilation, optimization, and technology mapping. Before doing the final stage of synthesis, FPGA pins (pad locations) have to be assigned accordingly to user guide. Notice that the (3) final synthesis for the integrated design would ignore the pin assignment of ADC_IN and DAC_DB since no analog input is involved in BPSK modulator, and only one DAC analog output is used for QAM modulated signal. Timing characteristics is an significant matter that affect the performance of FPGA implementation. The required path delay (estimated period) for Xilinx FPGA element should be less than the requested (constrained) clock period. Thus, timing slack (requested period − estimated period) should be positive value; otherwise the integrated design has to be redesigned. The clock frequencies used for the ADC/DAC SPI process and BPSK modulators (i.e. CLK_100 and LIO_CLKIN_1 or ADC_CLKOUT) are set to 100 MHz for both. The positive slack values in timing report generated by ISE of design synthesis in Table 2 is meet the timing requirement of FPGA constraint time. If any Xilinx IP (Intellectual Property) core is used in the integrated design, there will be another clock called System after clocks of CLK_100 and LIO_CLKIN_1.

Table (2): Timing Report of Design Synthesis

Constraint Clock	Requested		Estimated Period	Slack
	Frequency	Period		
CLK_100	100.0 MHz	11 ns	4.280 ns	3.720 ns
LIO_CLKIN_1	100.0 MHz	11 ns	3.404 ns	4.596 ns

Hardware Implementation

The Development board of Virtex-4 FPGA show in Figure 7 [13] offer a total development platform for designing and verifying applications based on the Xilinx family. This board enables designers to implement DSP and embedded processor based applications with extreme flexibility using IP cores and customized modules. The Virtex-4 FPGA along with Xilinx soft processor core makes it possible to prototype processor based applications, enabling software design teams early access to a hardware platform prior to working with the final product board. The board also supports the P240 expansion module standard, allowing application specific expansion modules to be easily added.

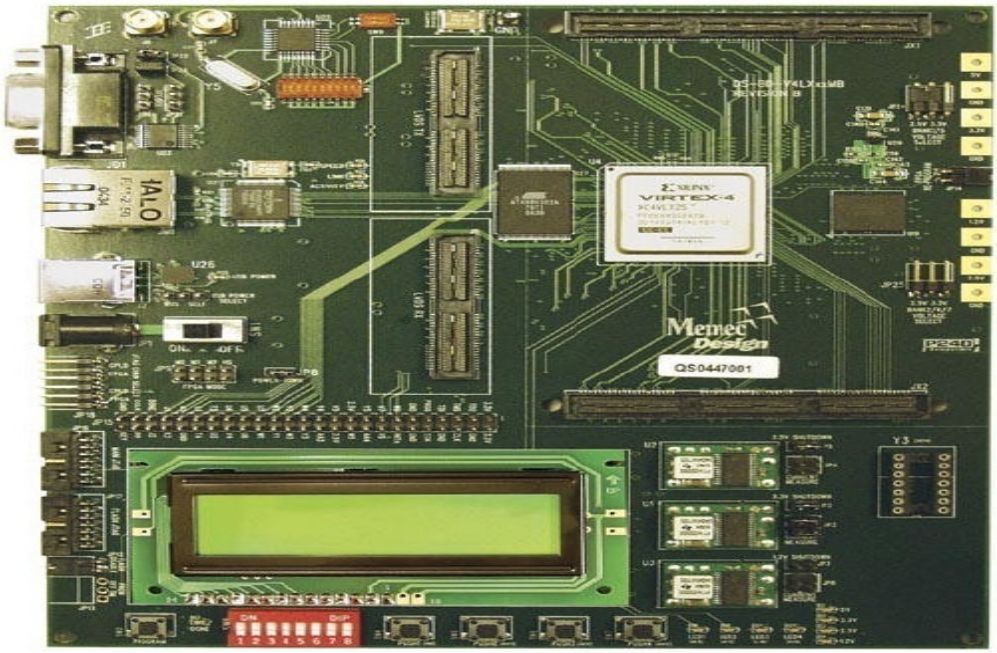


Figure (7): Virtex-4 System Board [13]

The Avnet P240 Analog Module [23] has 2 analog input and 2 analog output channels as show in Figure 8 provides an advanced analog interface to the Virtex-4 development board, featuring the Xilinx Virtex-4 FPGA. The Module enables dual-channel analog input and output functions for FPGA-based DSP applications, targeting communications, video, and general-purpose mixed-signal applications. The analog input channels are identical in design and include differential signal conditioning front ends. Texas Instruments ADS5500 14-bit, 125 MSPS A/D converters transform incoming analog signals into 14-bit data for the FPGA located on the baseboard. The 750 MHz analog input bandwidth of these devices makes them ideal for high intermediate-frequency (IF) or under sampling applications of signals into the UHF band. A Texas Instruments 16-bit, 500 MSPS, interpolating dual-channel DAC generates analog outputs. The DAC5687 features optional signal processing blocks including digital interpolation filters and quadrature modulation, all programmable via a serial interface port. The 50-ohm transformer coupled DAC outputs include analog reconstruction filter stages. The ADC input and DAC output signals in P240 Analog Module for the Proposed BPSK model are connected to oscilloscope in order to display real-time result. It should be noted that the empirical (real-time) result is identical to the simulated result.

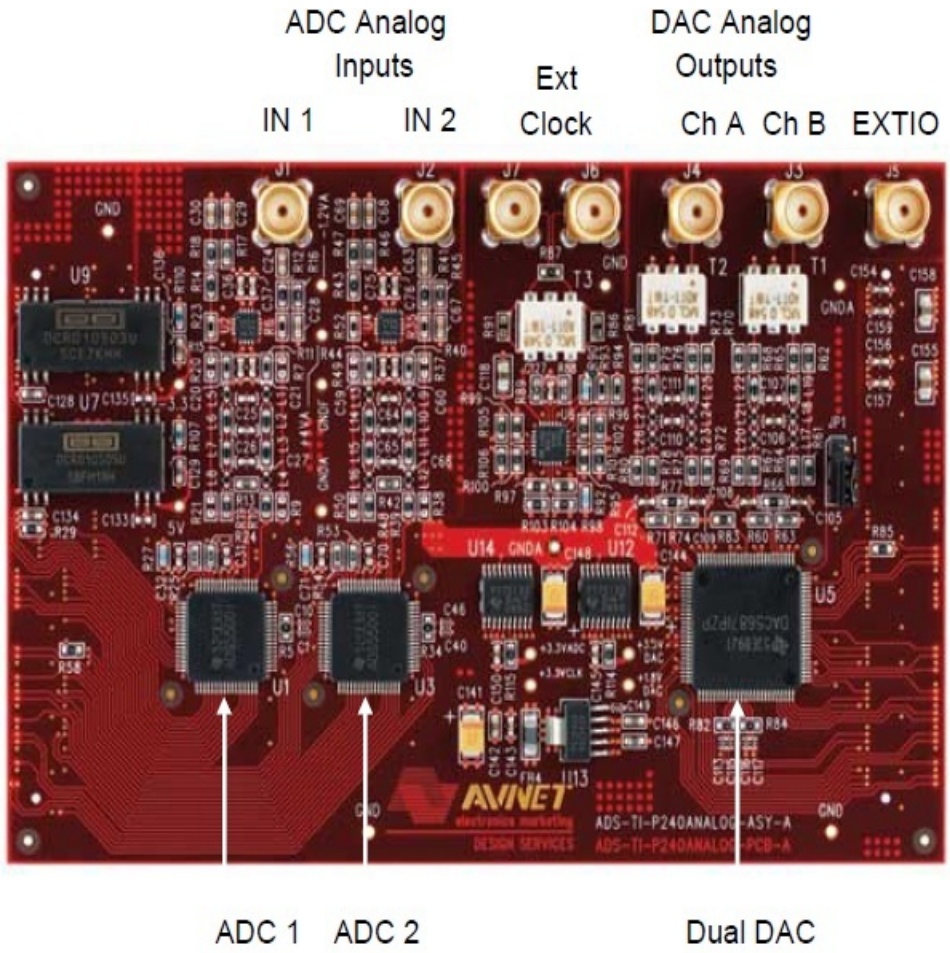


Figure (8): Avnet Electronics Marketing P240 Analog Module [23] .

The integrated modules of QAM model (with setup configuration) are implemented in Xilinx Virtex-4 Boards and P240 Analog Modules as illustrated in Figure 9. After completely downloading program of the integrated module from PC into Xilinx Virtex-4 FPGA through JTAG cable, the setup configuration module runs first. The sample rates of ADS5500 ADC and DAC5687 DAC (at *CLK2/C* pins) coming from the CDCP1803 are 100 MSps (= 400/4) and 400 MSps respectively.

In the nonappearance of mistake and caution for Design Rule Check (DRC) and bit-stream generation process, the configuration bit-stream file is downloaded to Virtex-4 FPGA board.

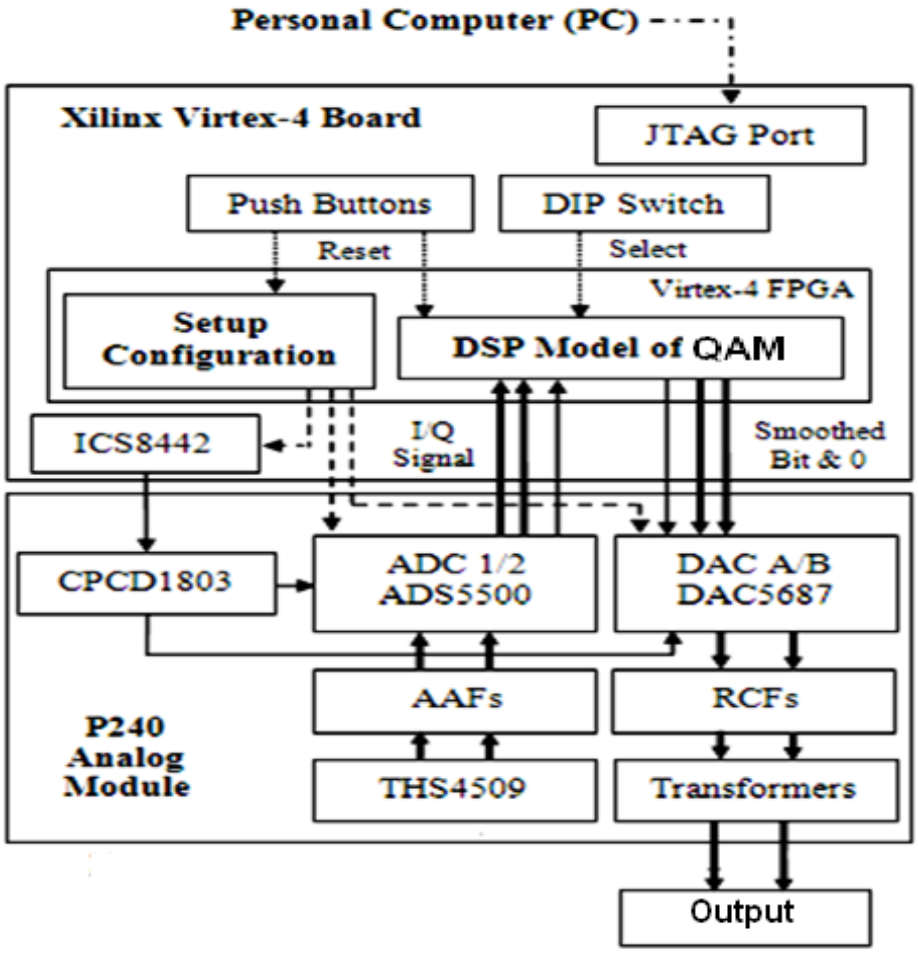


Figure (9): Hardware Implementation of FPGA and P240.

The device utilization for Virtex-4 FPGA after Map process is shown in Figure 10. As shown in the post PAR (final) static timing report in Table 3, the positive worst case slacks (constrained period – best case required period) fulfill the timing requirement. The maximum allowable sampling rate for QAM transmitter used in Virtex-4 FPGA is 206.6543 MSps (= 1/4.839 ns). However, the maximum sampling rate of LIO_CLKIN_1 from ADS5500 is 125 MSps; thus the maximum sampling rate of QAM transmitter that can be used in Virtex-4 FPGA MB development board with P240 Analog Module is 125 MSps.

Table (3): Post PAR Static Timing Report

Constraint Clock		Worst Case Slack (ns)		Best Case Required Period	Error
Name	Period	Setup	Hold		
CLK_100	11 ns	4.684	0.534	3.316 ns	0
LIO_CLKIN_1	11 ns	4.161	0.452	3.839 ns	0

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	952	9,312	7%	
Number of 4 input LUTs	679	9,312	10%	
Number of occupied Slices	765	4,656	16%	
Number of Slices containing only related logic	765	765	100%	
Number of Slices containing unrelated logic	0	765	0%	
Total Number of 4 input LUTs	1,101	9,312	11%	
Number used as logic	952			
Number used as a route-thru	149			
Number of bonded IOBs	39	232	16%	
Number of BUFGMUXs	3	24	12%	
Average Fanout of Non-Clock Nets	3.18			

Figure (10): Device utilization for Virtex-4 FPGA.

The DAC Channel A output from P240 Analog Module is connected to oscilloscope in order to display real-time result in analog domain. By observing the real-time result of QAM transmitted signal and simulated signal as shown in Figure 11. The real-time waveform characteristics of the QAM are compared with simulation waveform characteristics such as pulse interval (ns) and lower/higher amplitude peak as shown in Figure 11 and Table 4. The pulse interval of the real-time signal is 100 ns and the pulse interval of the simulated signal is likewise 100 ns. This means that no error difference is found between them. The timing error is satisfied because of accurate timing adjustment, whereas errors of 5% are found between the amplitude of real-time signal and the amplitude of simulated signal because of hardware constraints related to wiring, chip, and printed circuit board (PCB). However, the errors are acceptable. The real-time and simulated results in the time domain show equivalence in shape.

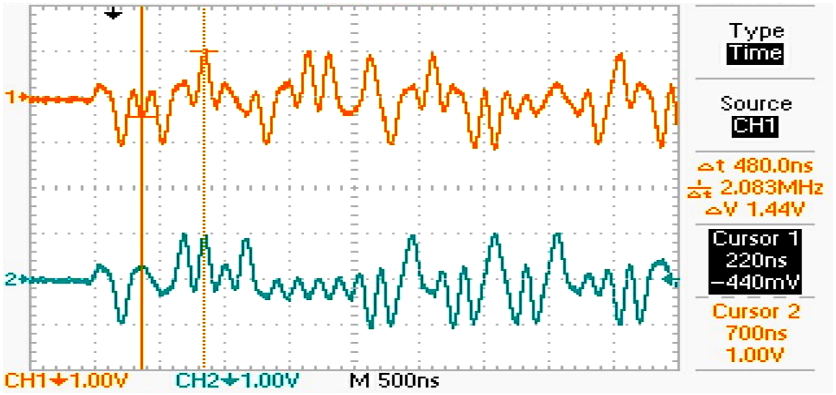


Figure (11): Real time and simulated waveforms.

Table (4): Comparison of real time and simulation results.

Waveform characteristics	Real time	Simulated	Difference	Error (%)
Pulse interval (ns)	100	100	0	0%
peak (v)	1.05	1.00	0.04	5%

Results Evaluation

Comparing with conventional design, the proposed reconfigure digital modulator look better performance and less FPGA area resulting in low power consumption . The resulting FPGA implementation in terms of Slices and LUTs is illustrated in Table 5.

Table (5): Resources comparison

Resources	[8] 2010	[17] 2009	Proposed Model 2013	Improvements
Slices	2922	2237	765	65%
LUTs	4674	3310	679	79%

CONCLUSION

This paper has presented the design and implement programmable modulators in Virtex-4 FPGA development board with DAC in P240 Analog Module. A lot of software and design tools have been used to verify the design output in terms of behavior, functionality, synthesis, timing, and area constraints. The comparison of empirical real-time and simulated results shows the success of FPGA and DAC implementations that would be further processed by external analog RF devices. The timing issues such as sample rate, constraints, and matching should be concerned in-depth if the input bit is coming from external source which is different from the presented design. Inserting pulse-shaping filtering between polar conversion and mixer can further reduce inter-symbol interference (ISI) to enhance the receiver performance. The HDL code of the QAM modulator is generated by Xilinx system generator and ModelSim. The proposed flow of FPGA design and implementation will gave better performance and accurate results with different modulation scheme with less utilization in slices and look up table (LUT) in near future if the researcher used shorter path and modern software to support the current and future communication system. The designed modulator could be consider suitable for being integrated into next generation high data rate wireless communication transceivers with low power consumption.

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