An Investigation of Electrical Properties of (p-n) Porous Silicon Layer

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Revised on: 17/10/2012 & Accepted on: 11/6/2013

ABSTRACT

In this work, we studied the electrical properties of (p-n) porous silicon layer under different etching time. The (p-n) porous silicon layer prepared by photo-electrochemical etching process. The dark I-V characteristics; give us rectification ratio with wide range as a function to etching time. A high value for the rectification behavior is related for etched samples at low etching time. While the increasing of etching time to high value show a non rectification behavior in (p-n) porous samples. The values of the photo-current for (p-n) porous sample at low etching time has very small value compared with the other (p-n) porous silicon samples at high etching time and this behavior in PSi layer in high etching time cannot be employed light emitting diode applications. While the layer prepared at low etching time is well suitable for light emitting device.

Keywords: (P-N) Porous Silicon, Electrical Properties of Psi, Photo-Electrochemical Etching.

التحقق عن الخصائص الكهربائية لـ (p-n) من طبقة السليكون المسامي

الخلاصة

في هذا البحث قمنا بدراسة الخصائص الكهربائية لطبقة السيليكون المسامي نوع (p-n) المحضر من طبقة السليكون المسامي بازمان تنميش مختلفة وبطريقة التنميش الكهروكيميائي-الضوئي (PEC). و من خلال منحنيات تيار- جهد بالظلام اعطى قيم تقويم عالية تمتلك قيم واسعة كدالة لزمن التنميش وخصوصاً عند ازمان تنميش قليلة. عند زيادة زمن التنميش لحد كبير ادى الى ظهور السلوك اللا تقويمي في عينات (p-n). ان قيم التيار- الضوئي عند ازمنة التنميش القليلة اعطى قيمة صغيرة جدا مقارنة مع القيم الاخرى عند زيادة زمن التنميش. لذا فان استخدام ازمنة تنميش عالية تولد لنا عينات (p-n) لاتصلح لعمل الثنائيات الباعثة لضوء على العكس مع ازمنة التنميش القليلة التي تصلح لانتاج الثنائيات الباعثة للضوء.

https://doi.org/10.30684/etj.31.7B.7
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INTRODUCTION

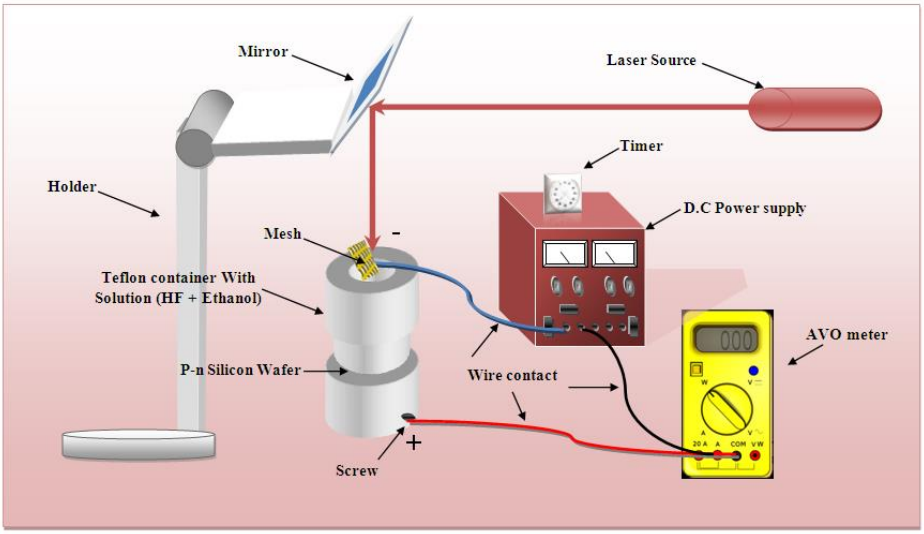
Over many years, the technological interest in PSi is essentially related to its extremely large surface-to-volume ratio and high tendency for oxidation [1]. It is unlikely that silicon will be replaced by another semiconductor in the foreseeable future. Although many of the components can be fabricated by this technology, PSi has been applied in a wide range of applications such as optoelectronic integrated circuits (OEIC), but this is beginning to change [2]. In optoelectronic [3], photovoltaic device and biomedical applications [3, 4], and more recently as templates for nanofabrication [5] and many others.

A variety of pore sizes ranging from a few nanometers up to a few micrometers can be obtained during the Si etching process, depending on different operating parameters including the concentration of HF in the electrolyte [6], the current density, the presence of a surfactant, type and density of silicon dopants and illumination process, whereas the etching time determines mainly the pore length [7, 8]. It is generally accepted that the electrochemical anodization in silicon/fluoride system is a self-limiting process and occurs only at the interface between PSi and crystalline Si substrate, and hence the already etched porous layer is unaffected by further electrochemical etching [9]. The porosity of the produced PSi layer can be controlled and modulated by adjusting the applied current and etching time.

In this work we study the electrical properties of (p-n) porous silicon layer as a function of etching time. Electrical properties were extracted using I-V and C-V characteristics measured in dark and under illumination intensity.

EXPERIMENTAL WORK

Porous silicon is fabricated from (p-n) silicon wafer of thickness (200)μm and of $(10^{17})cm^{-3}$ doping concentration for both accepter and donor region N_A and N_D, the resistivity of (0.125)Ω .cm for accepter and (0.0416)Ω .cm donor regions respectively. The silicon samples were $(1.5\times1)cm^2$. The etching process was carried out using photo-electrochemical etching process which employed (632.8) nm He: Ne laser with intensity (10.7) mW/cm^2 at different etching time (5, 15, and 20) min. The etching process was materialized in specially designed cell. This consists of two – electrode system as an anode and a mesh as cathode. The experiment was conducted in room temperature and is shown in the Figure (1). The cell provides us a porous silicon layer of uniform cross sectional area. This uniformity is recommended for the application of porous silicon and photovoltaic cells. The cross section of the home-made cell is shown in Figure (1), in which a mesh cathode with size aperture (1×1)mm was used. Figure (1) shows the Schematic diagram of the photo-electrochemical etching apparatus.



(a)

(b)

Figure (1) (a) The Schematic diagram of PEC system, (b) The photographic image of PEC system.

The electrical and photoelectrical properties of p-n porous silicon based device sandwiches (Al/p-n PSi/Al) porous silicon diode were studied. The Aluminum electrode on the porous layer covers a dimension of square area (4×4) mm^2. The measurements were carried out in a dark room and then under white light illumination conditions after etching process, using: A Kiethley – current source 2400 soft ware Lap view function

generator 50 HZ - was used to measure the flow current in dark condition at (0.1-5) V in forward and reverse biasing, at room temperature, The electrical measurements were carried out in the school of material engineering at the University Sains Malaysia in Penang.

Figure (2) shows the schematic diagram electrical measurements of voltage bias to I-V, C-V characterization.

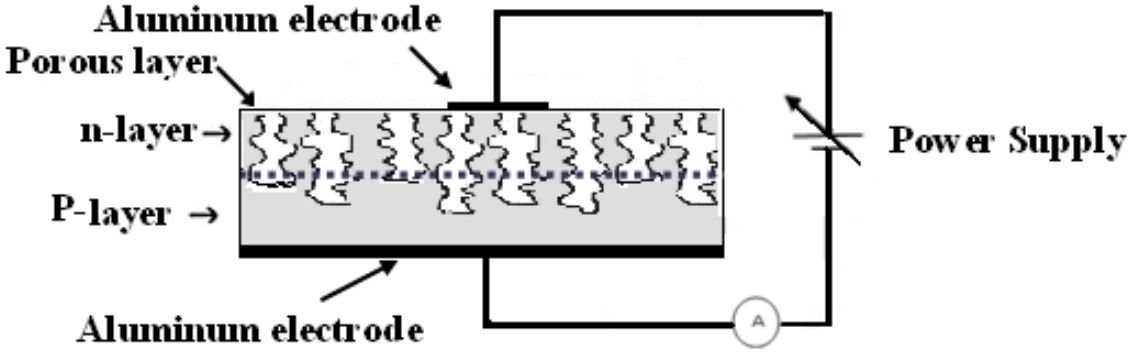


Figure (2) Schematic diagram electrical measurements.

The photo-current was measured for PSi after etching process. The photo-currents was carried out under light illumination intensity of (0.1) W/cm^2 and for forward and reverse cases.

RESULTS AND DISCUSSION

DARK CURRENT AND IDEALITY FACTOR

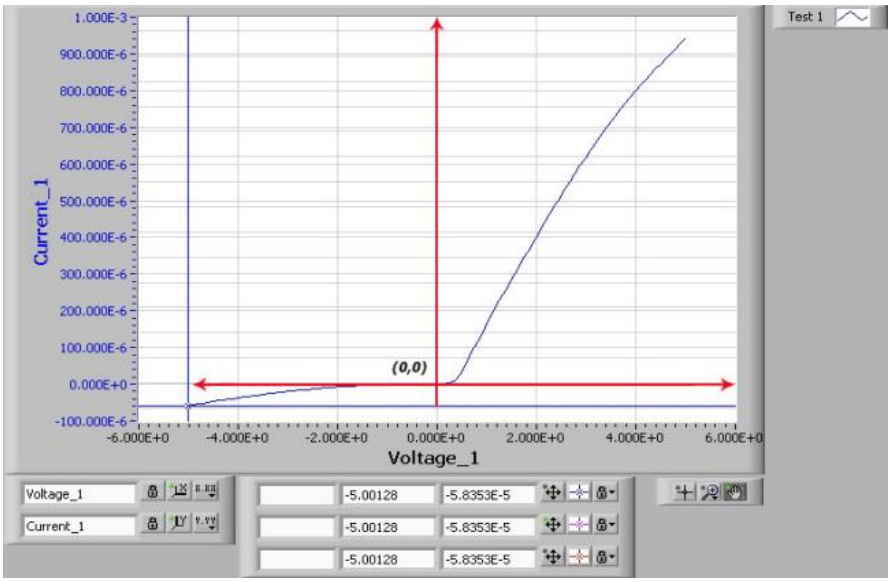
The I-V characteristic in dark, at room temperature with different bias voltage the range (0-5) V for (p-n) samples under etching time of (5, 15, 20) min and fixed illumination laser power density of (10.7)mW/cm^2 of etching process. As shown in figure (3a), (3b), (3c), the I-V characteristics the maximum rectification ratio of (17) at (5)min, (5) at (15)min and non rectifying in (20)min. This low a rectifying behavior may be due to the increasing of the density of state in porous silicon layer inside the (n-layer) which is known as dangling bonds [10, 11]. The density of this bond is increased with increasing the etching time [12]. The values of the rectification ratio (a) were calculated according the equation (1) [10]:

$$a = I_{F\,max} / I_{rev\,min} \qquad \ldots (1)$$

For (Al/p-n PSi/ Al) measuring in dark room with different etching time. [10]
This curve give us good explanation for the case of the efficient light – emitting device (light emitting porous silicon) LEPsi. The (p-n) junction exhibited near exponential J-V characteristics:

$$J=J_o \exp(eV/nKT) \quad \text{.... (2)}$$

Where (K) is a Boltzman constant, (T) is the temperature, (J_o) is the saturation current density, and (n) is the ideality factor [10, 13].



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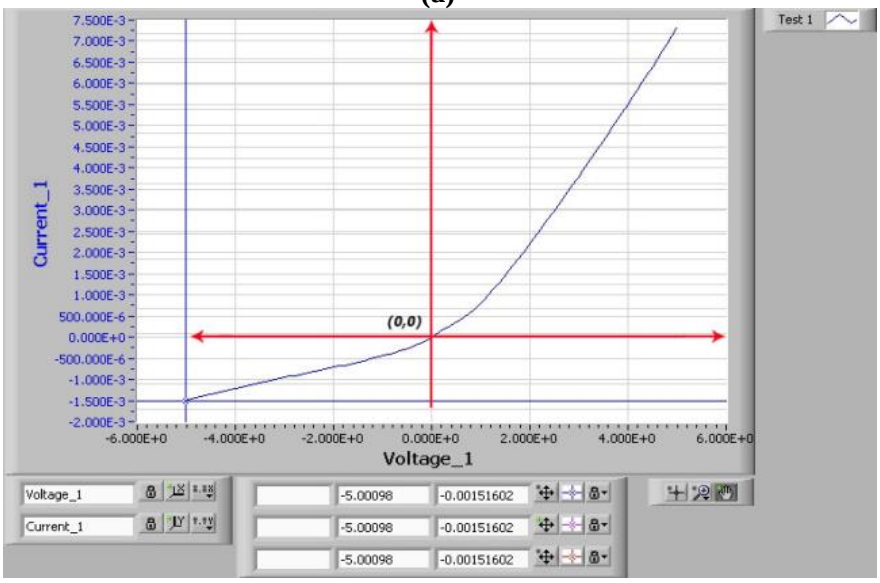

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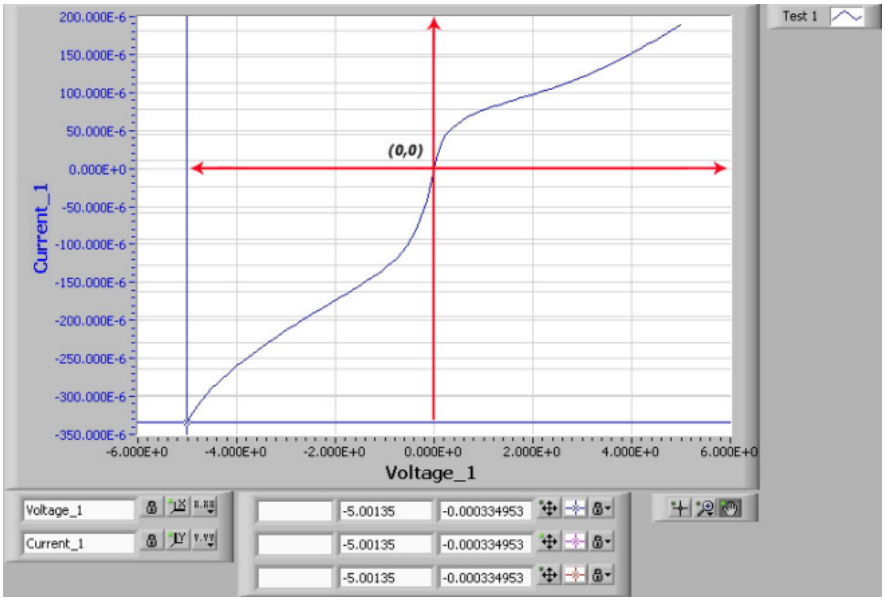
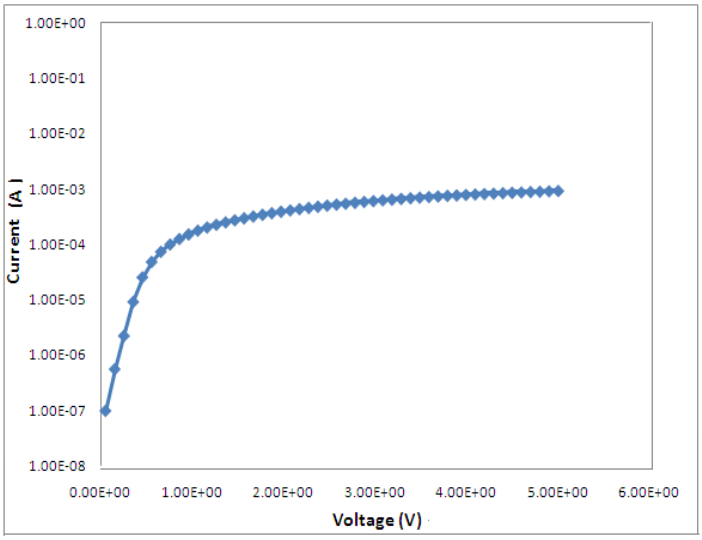


(c)

Figure (3) I -V characteristic of Al/p-n PSi/ Al measuring in dark Prepared with different etching time.



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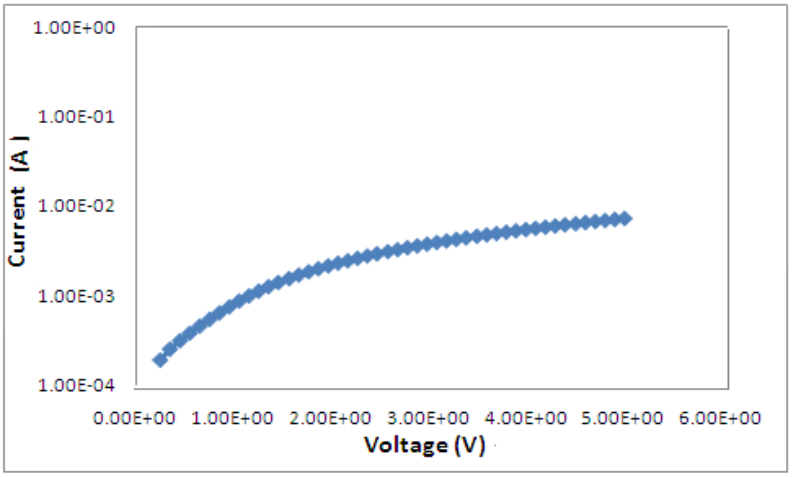

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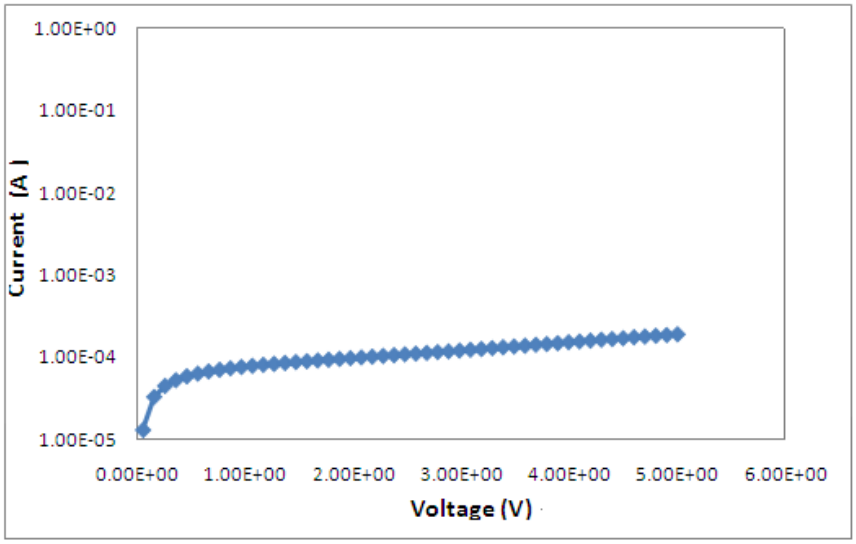


(c)

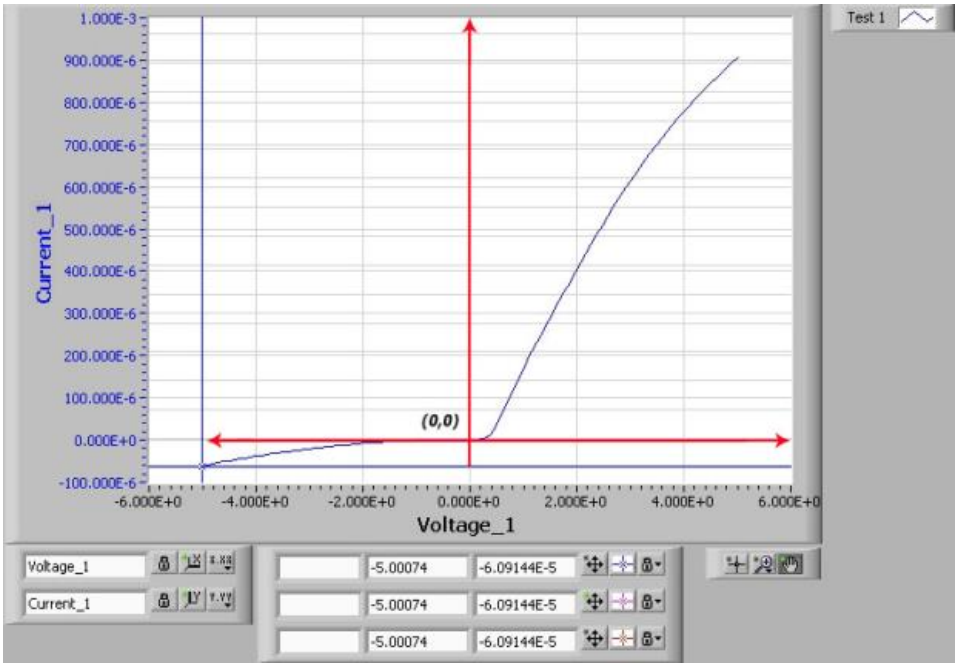
Figure (4) Semi log I -V characteristic of p-n porous silicon Junction measuring in dark prepared with Different etching time.

Figure (4a, 4b, 4c) presents the semi-log I-V plots in the dark room measurements, the I-V curve (linear–relationship) with ideality factors (3.5, 16, and 9) for etching time (5, 15, and 20) min respectively. The important electrical characteristic for a schottky like junction (PSi) can be calculated from equation (2) I-V measurement, like ideality factors (n): [14, 10].

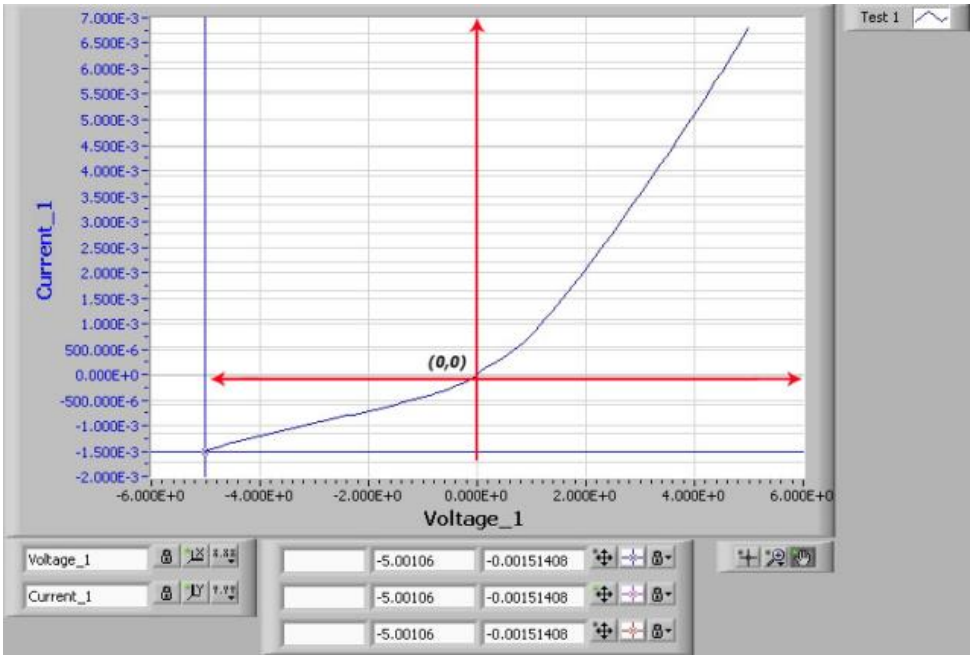
$$n = \frac{q}{K_B T} \frac{\Delta V}{\ln \frac{I}{I_s}} \quad \ldots (3)$$

PHOTO-CURRENT

The relationship between the reverse bias voltage and the photo-current (I_{Ph}), where ($I_{Ph}= I_{Total}- I_{dark}$) of (p-n) porous silicon is shown in Figure (5a,5b,5c) the photo-urrent at reverse biasing of (5)V is about (2×10^{-5})A at (5)min, increasing photocurrent to the value (6×10^{-4})A at (15)min, while I_{Ph} is about (6×10^{-6})A at etching time (20)min [15], this referring to the fact that the density of radiative and / or non - radiative recombination process between the electrons and holes has a minimum value [2].



(a)



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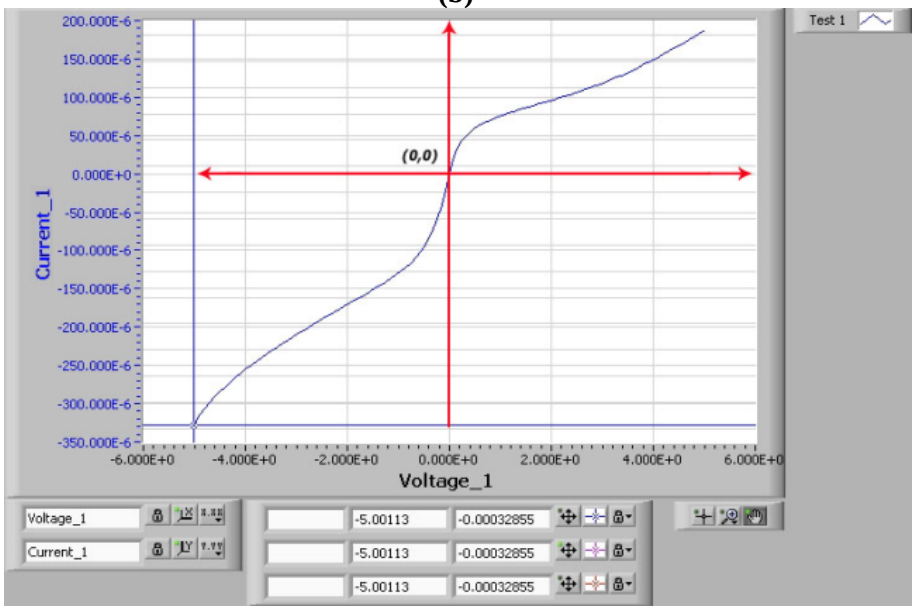


(c)

Figure (5) I -V characteristic of Al/p-n PSi/ Al measuring under illumination intensity of (0.1) W/cm^2 prepared with different etching time.

CAPCITANCE-VOLTAGE CHARACTERISTICS

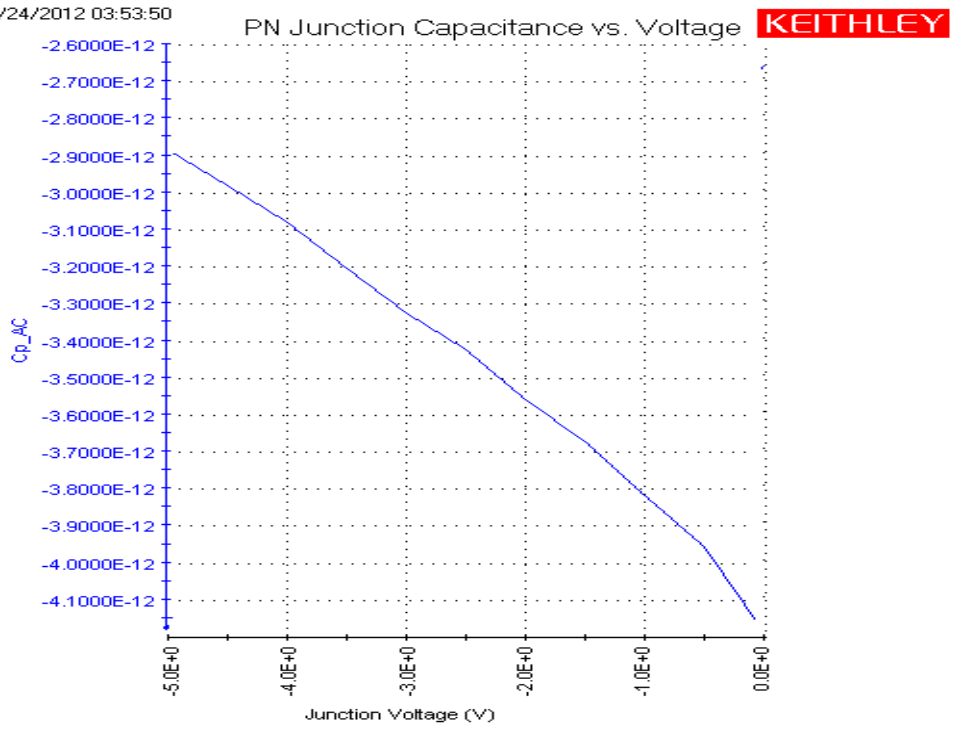
The capacitance-voltage characteristics of Al/p-n PSi/Al structures depend on the morphology and the porosity of the etched silicon surface in a addition to the layer thickness [16, 17]. Figures (6a,6b and 6c); shows the (C-V) characteristics under different

reverse biasing ranging from (0-5)V at different etching time of (5, 15, 20)min respectively, capacitance of the porous structure in Figure (6c) It is found that the formation of fully penetrate porous silicon layer can lead to nearly constant in the high etching time and doesn't response for the variation in applied reverse voltage [18], and this behavior conform that the total capacitance is a series combination as stated in equation (4) [19], while for the case of Figure (6a and 6b); the capacitance are decreased with increasing the applied reverse voltage but does not give us a linear relationship between C^{-2} or C^{-3} with the applied reverse voltage. May be attributed to an increasing holes number on the silicon surface with increasing the etching time which in turns lead to a preferential dissolution between nearest - neighbor's pores which promotes the pore-pore overlap [18].

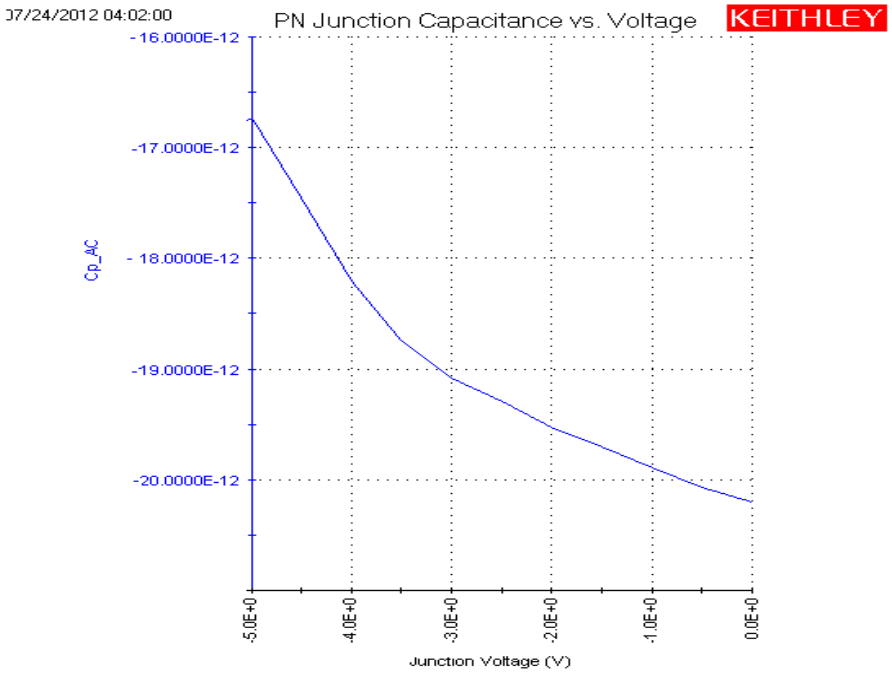
And in this case the result is series combination between the junction capacitance and PSi layer capacitance. The capacitance of the junction is much important that the PSi capacitance, according to the equation (4). When the size of crystalline silicon is decreased to a level at which quantum confinement effects appear, the energy band gap is increased.

$$\frac{1}{C_T} = \frac{1}{C_J} + \frac{1}{C_{layer}} \qquad \text{... (4)}$$

Where C_{layer} is the porous silicon capacitance and the C_J is the other capacitance especially the junction capacitance.



(a)



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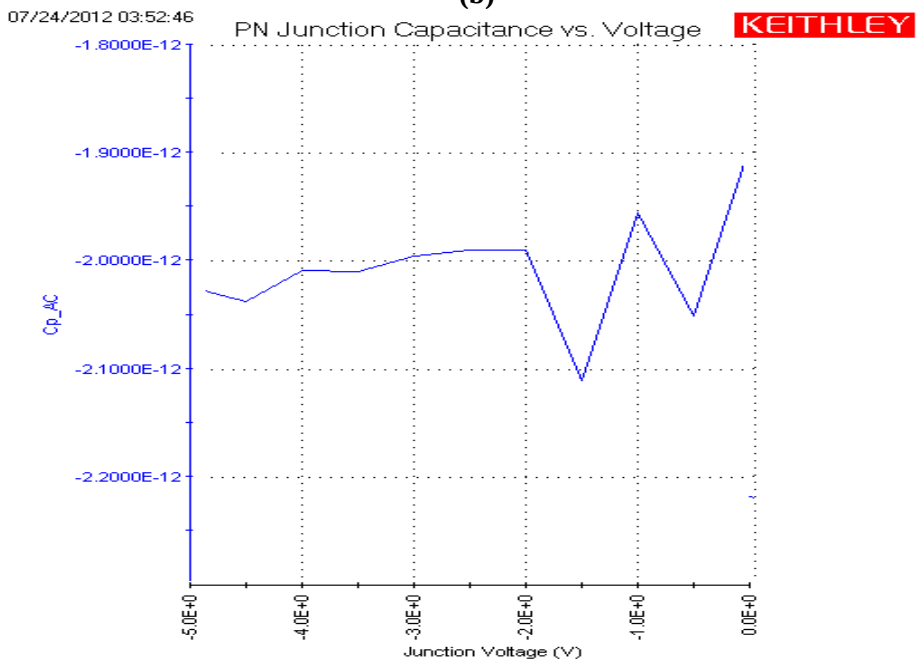

(c)

Figure (6) the capacitance-voltage characteristics of (p-n) PSi layer Which prepared with different etching time.

CONCLUSIONS

The I-V characteristics of (p-n) porous sample at (5) min etching time show good rectifying behavior with maximum rectification ratio of about (17) at (5)V. Compare with the other (p-n) porous samples prepared at high etching time. The reduction in rectifying behavior with increasing etching time, is due to the increasing of the density of state in porous silicon layer inside the (n-layer) which is known as dangling bonds. The value of the photo-current for (p-n) porous sample at low etching time has very small value compared with the other (p-n) porous silicon samples prepared at high etching time and this layer can be used for perpetration of light emitting (p-n) porous rather than photo conductive and photovoltaic devices. The value of the photo-current for (p-n) porous samples at high etching time is higher than the other samples at low etching time and the resulting porous layer can act as a effective material for photovoltaic or photo conductive devices. The porous silicon of high illumination intensity and characteristics has lower photo-current and hence can be regarding of (LEPSi) not photo voltaic porous silicon.

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