I-V and C-V Characteristics of Porous Silicon Nanostructures by Electrochemical Etching

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ABSTRACT

Porous silicon (PS) layers has been prepared in this work by electrochemical etching (ECE) technique of a p-type silicon wafer with resistivity (1.5-4 Ω.cm) in hydrofluoric (HF) acid of 20% concentration. Various affecting studied etching time (10, 30, and 45 min) and current density (15 mA/cm^2). We have study the morphological properties (AFM) and the electrical properties (*I-V* and *C-V*).

The atomic force microscopy investigation shows the rough silicon surface, with increasing etching process (etching time) porous structure nucleates which leads to an increase in the depth and width (diameter) of surface pits. Consequently, the surface roughness also increases.

The electrical properties of prepared PS; namely current density-voltage characteristics under dark, show that the pass current through the PS layer decreased by increasing the etching time, due to increase the resistivity of PS layer. The PS layer shows a rectifying behaviour with different rectification ratio. *C-V* measurements shows that the increase of the etching time decreases the capacitance of the PS layer. This behavior was attributed to the increasing in the depletion region width which leading to the increasing of built-in potential.

Keyword: Anodization; porous silicon; Morphological properties; Electrical properties.

خصائص (تيار- فولتية) و (سعة - فولتية) للسليكون المسامي نانوي التركيب بالتنميش الكهروكيمياوي

الخلاصة

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في هذا البحث، تم تحضير السليكون المسامي بتقنية التنميش الكهروكيميائي لشريحة سليكون من النوع (p) بمقاومية (١,٥-٤ أوم.سم)، باستخدام حامض الهيدروفلوريك بتركيز ٢٠%. جرى دراسة تاثير ازمان تنميش مختلفة (١٠، ٣٠ و ٤٥ دقيقة) وكثافة تيار (١٥ ملي امبير/سم^2). تم دراسة الخصائص الطبوغرافية (AFM) والكهربائية (*I-V*) و (*C-V*) لطبقة السليكون المسامي .

أظهرت فحوصات مجهر القوى الذري على سطح سليكون خشن ، مع زيادة عملية التنميش (زمن التنميش) نوى البنية المسامية الذي تؤدي إلى زيادة في عمق وعرض (القطر) من حفر السطح. وبالتالي فإن الزيادة بخشونة السطح أيضا تزداد.

الخصائص الكهربائية لطبقة السليكون المسامي المحضرة؛ اي خصائص تيار - جهد تحت الظلام، أظهرت ان التيار المار خلال طبقة السليكون المسامي يقل بزيادة زمن التنميش، نتيجةً لزيادة مقاومية طبقة السليكون المسامي. أوضحت طبقة السليكون المسامي سلوكاً تقويمياً مع نسب تقويم مختلفة. أظهرت قياسات سعة - جهد ان بزيادة زمن التنميش تقل سعة طبقة السليكون المسامي. هذا السلوك يعزى الى الزيادة في عرض منطقة الاستنزاف التي تؤدي الى زيادة في جهد البناء الداخلي.

INTRODUCTION

Porous silicon consists of nanometer- and micrometer-sized pores. The nanoporous layer has attracted considerable attention due to its visible light emissions [1].

The optical or electrical properties of porous silicon (PS) single layers have been used in many chemical and biological sensing applications due to the large specific surface area of the material (200-800 m^2/cm^3) [2].

The porous silicon structure is formed by electrochemical etching of Si wafers in electrolytes including hydrofluoric acid (HF) and surfactants (mainly ethanol). Ethanol is often added to facilitate evacuation of H_2 bubbles; these bubbles can easily leave the surface because of the decreased surface tension of the liquid. Additionally, the bubbling enhances the liquid circulation in the electrolyzation cell, which helps the transport of reactants and side products. To be able to synthesize uniform layers with high reproducibility, the applied anodic current density and etching time are monitored, controlled and kept at a particular constant level required during the process [3].

Porous silicon (PS) (Uhlir, 1956) was first developed in the 1950s and exhibits unique optical and electrical properties due to quantum confinement effects (Canham, 1990; Cullis et al., 1997). Porous silicon is easily produced by electrochemical etching in a solution of hydrofluoric (HF) acid, and the pore diameter can be controllably varied from a few nanometers up to several hundred nanometers by adjusting the etching parameters (Herino et al., 1987; De Stefano et al., 2004) [4].

Electrochemical etching with respect to *I-V* curve should be well accurate to observe the pore nucleation and growth. Correlation of the current oscillations with morphological changes of oxide layer should help in explanation of its formation

mechanism. Potentials were the initial pore formation and electropolishig occurs plays a major role in silicon electrochemistry. Preparation of Si with desired morphology results in more accurate properties and applications [5].

Different morphologies and size of the pores reflects a difference in etching conditions. The more important parameters are the type and the level of doping atoms, crystal orientation, electrolyte composition, and conditions of anodizing, design of Etching chamber, preparation of silicon surface before and after electrochemical etching. These factors cause that samples prepared in different laboratories can be no comparable, even at comparable experimental conditions [6].

EXPERIMENTAL PROCEDURE

Samples used in this study are boron doped crystalline silicon (c-Si) wafers (thickness 508±15μm and resistivity 1.5-4 Ω.cm) grown by Czochralski (CZ) method in (111) orientations. AFM the atomic force micrographs were taken for porous silicon by AA3000 Scanning Probe Microscope Angstrom Advanced Inc.

The porous samples were then prepared by electrochemical anodic dissolution of doped silicon in 40% hydrofluoric acid and ethanol with gold electrode as cathode. The electrolyte was prepared by mixing HF (40%) and ethanol in 1:1ratio. The wafer and the solution were placed in a Teflon cell as shown in Figure (1). The porous layers on the surface of these samples were prepared at current density 15 mA/cm^2 with etching times of 10, 30 and 45 min.

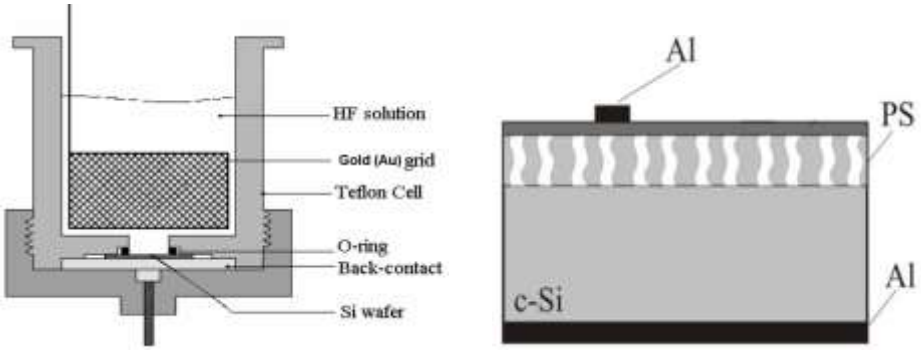


Figure (1)) a) Schematic diagram of the porous silicon anodization (b)Schematic image of Al/PS/Si/Al structure.

RESULTS AND DISCUSSION

a) Morphological Properties

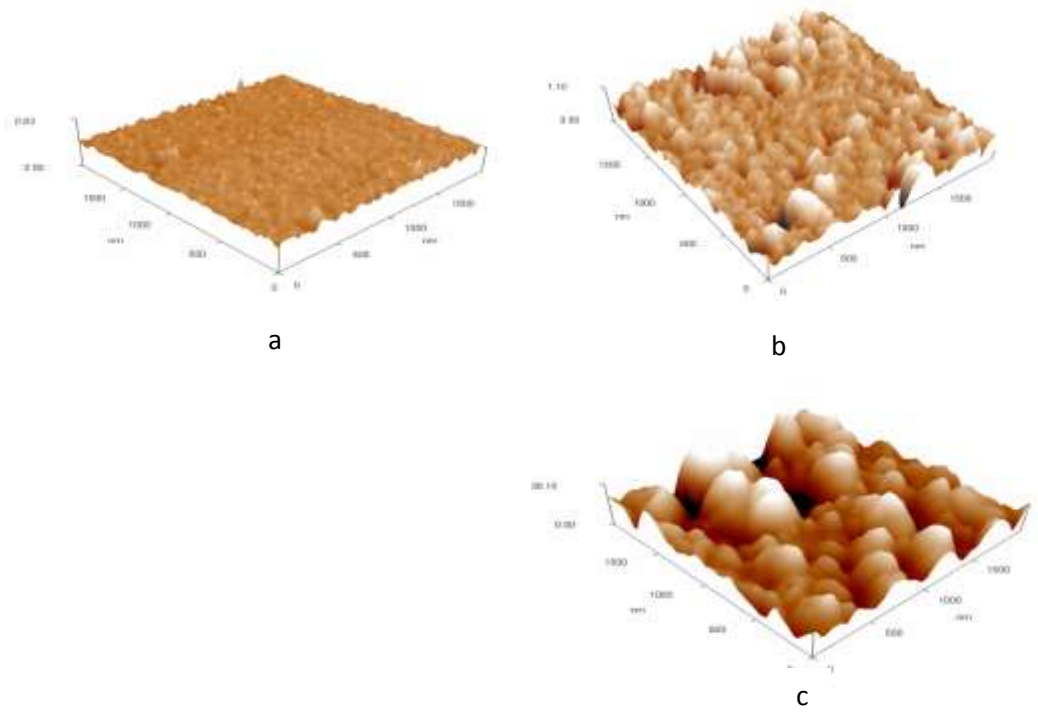
When etching time increases a part of pores coagulate to larger structures. Figure (2) distributed nanocrystalline silicon pillars and voids over the entire surface can be seen. with increasing etching process (etching time) porous structure nucleates which

leads to an increase in the depth and width (diameter) of surface pits. Consequently, the surface roughness also increases.

Table (1) gives the roughness average, root mean square and diameter average.

Table (1) the calculated morphology characteristics of PS samples prepared With different etching process.

Current density (mA/cm^2)	Etching Time (min)	Roughness Ave. (nm)	RMS (nm)	Ave. Diameter (nm)
15	10	0.462	0.656	41.65
	30	0.936	1.19	39.88
	45	6.93	8.84	128.85



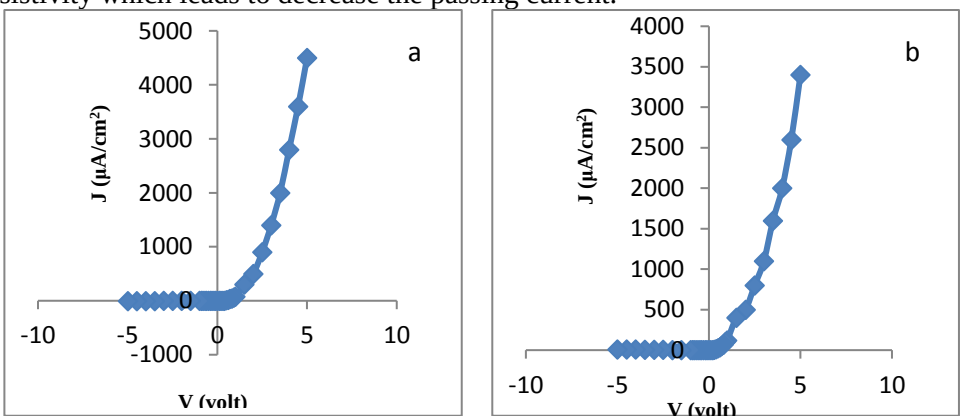
a b c

Figure (2) 3D AFM image of porous silicon prepared at J=15 mA/cm^2 etched under different etching time (a) 10, (b) 30 and (c) 45 min.

b) I - V characteristics

Figure (3) shows a typical diode behavior can be seen. It shows the Current density-Voltage (*J-V*) characteristics of Al/PS/p-Si/Al sandwich structure device prepared at current density 15 mA/cm^2, with different etching time (10, 30 and 45 min.). The *J-V* curves were obtained by applying a varying the applied bias (sweeping from −5 V to +5 V) and then measuring the resulting current.

By increasing the etching time from 10 to 45 min., we showed have smaller current passing through the PS layer with the same applied voltage. This decreasement reflects the fact which is, increasing the etching time leads to increase the porosity and then the resistivity which leads to decrease the passing current.



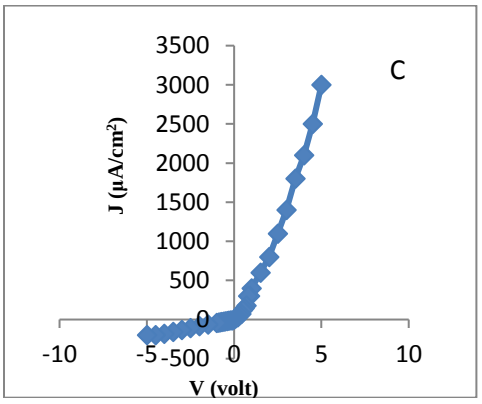


Figure (3) Dark, forward bias and reverse bias *I –V* characteristics of PS 15 mA/cm^2 at etching time 10 (b) 30 (c) 45 min.

c) C - V characteristics

C-V characteristics of Al/PS/p-Si/Al sandwich structure device depend on the morphology and the porosity of the etched silicon surface. Figure (4) shows the *C-V* characteristics of the sandwich structure (Al/PS/*p*-Si/Al) with different etching time (10,30 and 45 min.), and constant current density (15 mA/cm^2)

The effect of the etching time on the *C-V* characteristics is studied. Results in Figure (4), it shows that the increase of the etching time decreases the capacitance of the

PS layer. This behavior was attributed to the increasing in the depletion region width which leading to the increasing of built-in potential.

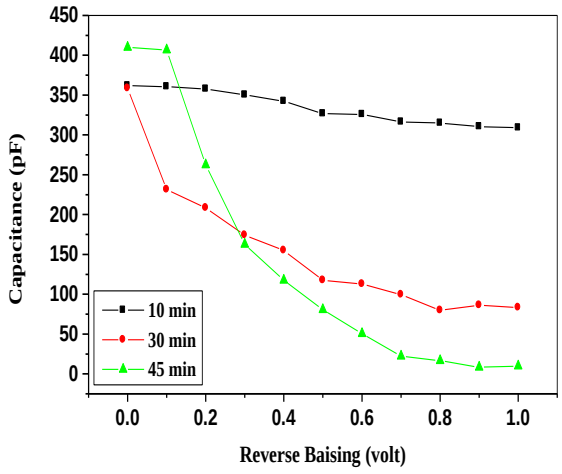


Figure (4): The Capacitance -Voltage characteristics for different etching Times 10, 30 & 45 min, and current density 15 mA/cm^2.

CONCLUSIONS

1. The atomic force microscopy investigation shows the rough silicon surface which can be regarded as a condensation point for small skeleton clusters which plays an important role for the characterized the nanocrystalline porous silicon.
2. The electrical properties study reveals that to:

- The porous layer resistivity is much larger than that for crystalline silicon and this resistivity increases with increasing the etching time.
- The *C-V* characteristics shows that the increase of the etching time decreases the capacitance of the PS layer. This behavior was attributed to the increasing in the depletion region width which leading to the increasing of built-in potential.

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