

A Multiplier-less Implementation of Two-Dimensional Circular-Support Wavelet Transform on FPGA

Jassim M. Abdul-Jabbar, Zahraa Talal Abede and Akram A. Dawood
drjssm@gmail.com zah_ta84@yahoo.com akram.dawood80@gmail.com

Department of Computer Engineering, College of Engineering, University of Mosul, Mosul, Iraq.

Abstract:

In this paper, a two-dimensional (2-D) circular-support wavelet transform (2-D CSWT) is presented. 2-D CSWT is a new geometrical image transform, which can efficiently represent images using 2-D circular spectral split schemes (circularly-decomposed frequency subspaces). 2-D all-pass functions and lattice structure are used to produce 1-level circular symmetric 2-D discrete wavelet transform with approximate linear phase 2-D filters. The classical one-dimensional (1-D) analysis Haar filter bank branches $H_0(z)$ and $H_1(z)$ which work as low-pass and high-pass filters, respectively are transformed into their 2-D counterparts $H_0(z_1, z_2)$ and $H_1(z_1, z_2)$ by applying a circular-support version of the digital spectral transformation (DST). The designed 2-D wavelet filter bank is realized in a separable architecture. The proposed architecture is simulated using Matlab program to measure the deflection ratio (DR) of the high frequency coefficient to evaluate its performance and compare it with the performance of the classical 2-D wavelet architecture. The correlation factor between the input and reconstructed images is also calculated for both architectures. The FPGA (Spartan-3E) Kit is used to implement the resulting architecture in a multiplier-less manner and to calculate the die area and the critical path or maximum frequency of operation. The achieved multiplier-less implementation takes a very small area from FPGA Kit (the die area in 3-level wavelet decomposition takes 300 slices with 7% occupation ratio only at a maximum frequency of 198.447 MHz).

Keywords: 2-D circular-support wavelet transform, Circular split 2-D spectral schemes, 2-D circular Haar filter, Wavelet transform, Lattice structure, IIR filter, Haar filter,

بناء التحويل المويجي المدور ذي البعدين على شريحة FPGA بدون مضارب

أ.د. جاسم محمد عبد الجبار و زهراء طلال عبد المختار و أكرم عبدالموجود داود

قسم هندسة الحاسوب - كلية الهندسة - جامعة الموصل - الموصل - العراق

الخلاصة:

في هذا البحث، سيتم تقديم التحويل المويجي ذي البعدين المدور. إن التحويل المويجي ذا البعدين المدور هو احد التحويلات الهندسية الجديدة للصور والذي يمكنه تمثيل الصورة بشكل كفؤة باستخدام مخطط فصل طيفي مدور ذي بعدين وسيتم استخدام دوال الإمرار الكلي ذوات البعدين (2-D all-pass functions) و الهيكل المتشابك (lattice structure) لتوليد مستو واحد من التحويل المويجي المقطع ذي البعدين المدور المتمثل بمرشحات ذوات بعدين وبطور خطي تقريبي. إن مشرحي التحليل Haar التقليديين ذوات البعد الواحد $H_0(z)$ و $H_1(z)$ اللذان يعملان كفرعين لمرشحي الترددات الواطئة والعالية لجرف المرشح، على التوالي سيتم تحويلهما الى مرشحين ذواتي بعدين $H_0(z_1, z_2)$ و $H_1(z_1, z_2)$ بتطبيق النمط المدور للتحويلات الطيفية (DST). إن المرشحات المويجية المقطعة ذوات البعدين والمصممة في هذا البحث سيتم تحقيقها باستخدام المعمارية المنفصلة. إن المعمارية ذات البعدين المقترحة سيتم تمثيلها ومحاكاتها باستخدام برنامج الـ Matlab لقياس نسبة الانحراف (deflection ratio) (DR) لمعاملات التردد العالي لتقييم إداء المنظومة ومقارنتها مع أداء المعمارية التقليدية للتحويل المويجي ذي البعدين التقليدي. كما حسب معامل الترابط بين الصور الداخلة والمسترجعة للمعماريتين. لقد تم استخدام مصفوفة البوابات المبرمجة حقيقياً (Spartan-3E FPGA) لتنفيذ المعمارية الناتجة بدون مضارب وكذلك لحساب المساحة المطلوبة للمعمارية ومعرفة المسار الحرج أو أعلى تردد للعمل. إن التنفيذ المنجز بدون مضارب يأخذ مساحة صغيرة جداً من الـ FPGA (المساحة المطلوبة لثلاث مستويات من المعمارية تأخذ 300 slices ونسبة إستغلال 7% كما إن أعلى تردد وصل الى 198.447 MHz).

1. Introduction

The multi-dimensional (M-D) signal processing has many applications in modern-day devices and softwares. Specifically, the two-dimensional (2-D) signal processing and analysis has evoked a lot of interest among researchers due to their numerous advantages in areas such as image processing [1], [2]. The 2-D filters are being widely used for various types of

processing and analysis. The main objective of this paper is to introduce 2-D filter functions using circular symmetry filters with lattice structures and implement them as wavelet filter banks in a separable manner.

Although the wavelet transform (WT) is known to be a powerful tool in many signal and image processing applications such as compression, noise removal, image edge enhancement, and extraction;

wavelets are not optimal in capturing the two-dimensional singularities found in images and often required in many segmentation and compression applications [3] – [5]. In particular, natural images consist of edges that are smooth curves which cannot be captured efficiently by the wavelet transform. Therefore, several new transforms are required for image signals. One of the recent transformations is the 2-D elliptical-support wavelet transform (2-D ESWT) which is used as the main feature extracting part in an efficient method for iris recognition [6].

A 2-D circular-support wavelet transform (2-D CSWT) is proposed in this paper as a new geometrical image transform, which can efficiently represent images using circular split 2-D spectral schemes (circularly - decomposed frequency subspaces). Such schemes are known to give better performance than rectangular-support schemes when it is desired to extract as low frequency information as possible in a 2-D low-pass filtering channel and as high frequency information as possible in a 2-D high-pass filtering channel [7]. The corresponding 2-D wavelet filters are designed. Then a multiplier-less implementation of such 2-D CSWT on FPGA is proposed. Experimental results are to be obtained to show the feasibility of the proposed implementation. These

results are also to be compared to the classical 2-D wavelet implementation method.

Several architectures for single-chip implementations of the 1-D DWT was described in the literature [8] – [11]. Each of these architectures was designed to compute the DWT in real time by interleaving computation. These architectures differed mainly in the method of storing and routing the intermediate results [12]. Those implementations included systolic routing networks, RAM based architectures [13], distributed memory [14], and implementations using minimum number of registers [15]. None of them utilized improvements available at the algorithmic level. In this paper, the implementation of 2-D discrete wavelet transform (2-D DWT) is considered by using digital filters $H_0(z_1, z_2)$ and $H_1(z_1, z_2)$ as a lattice structure of Haar filter.

This paper is organized as follows: In section 2, the characteristics of Haar filter are reviewed. The design of the proposed 2-D circular-support wavelet transform is introduced in section 3. In section 4, the performance and implementation results on FPGA are given. The values of some objective assessment parameters are computed in section 5. Finally, section 6 concludes this paper.

2. Haar Wavelet Transform

A 1-D Haar wavelet is the simplest type of wavelet filters. In discrete form, Haar wavelets are related to a mathematical operation called the Haar transform. The Haar transform serves as a prototype for all other wavelet transforms. As all wavelet transforms work, the Haar transform decomposes a discrete signal into two sub-signals of half its length. One sub-signal is a running average or trends; the other is a running difference or fluctuations. The 1-D Haar wavelet transform has a number of advantages [16]:

- It is conceptually simple.
- It is fast.
- It is memory-efficient, since it can be calculated in place without a temporary array.
- It is exactly reversible without the edge effects that are a problem with other wavelet transforms.

Haar 2-tap wavelet is chosen as a reference filter for the architecture of 2-D filter bank. The coefficients of the low-pass h_0 and the high-pass h_1 decomposition filters corresponding to this wavelet type are shown in Table 1 [7].

Table 1- Haar 2-tap wavelet coefficients.

h_0	h_1
$1/\sqrt{2}$	$1/\sqrt{2}$
$1/\sqrt{2}$	$-1/\sqrt{2}$

3. The Proposed 2-D Filter Bank

In this paper, a 2-D filter is proposed depending on the 1-D FIR Haar filter using the 1-D to 2-D Digital Spectral Transformation (DST) which given by [17]

$$z^{-1} \xrightarrow{\text{DST}} \left(\frac{a+z_1^{-1}}{1+az_1^{-1}} \right) \left(\frac{b+z_2^{-1}}{1+bz_2^{-1}} \right) \quad (1)$$

DST is used to convert the low-pass Haar filter in analysis stage into a 2-D version as in the following equations:

$$H_0(z) = \frac{1}{\sqrt{2}} + \frac{1}{\sqrt{2}} z^{-1} \quad (2)$$

By applying the DST technique, the low-pass Haar analysis filter can then be represented by two 1-D 1st order all-pass digital filter sections as follows:

$$\begin{aligned} \therefore H_0(z) &= \frac{1}{\sqrt{2}} (1 + z^{-1}) \\ \therefore H_0(z_1, z_2) &= \frac{1}{\sqrt{2}} \left(1 + \left(\frac{a+z_1^{-1}}{1+az_1^{-1}} \right) \left(\frac{b+z_2^{-1}}{1+bz_2^{-1}} \right) \right) \\ &\cdot \frac{1}{\sqrt{2}} \left(1 + \left(\frac{a+z_1^{-1}}{1+az_1^{-1}} \right) \left(\frac{b+z_2}{1+bz_2} \right) \right) \\ &\cdot \frac{1}{\sqrt{2}} \left(1 + \left(\frac{a+z_1^{-1}}{1+az_1^{-1}} \right) \right) \cdot \frac{1}{\sqrt{2}} \left(1 + \left(\frac{b+z_2^{-1}}{1+bz_2^{-1}} \right) \right) \\ &= \frac{1}{4} \left(1 + \left(\frac{a+z_1^{-1}}{1+az_1^{-1}} \right) \left(\frac{b+z_2^{-1}}{1+bz_2^{-1}} \right) \right) \\ &\cdot \left(1 + \left(\frac{a+z_1^{-1}}{1+az_1^{-1}} \right) \left(\frac{b+z_2}{1+bz_2} \right) \right) \\ &\cdot \left(1 + \left(\frac{a+z_1^{-1}}{1+az_1^{-1}} \right) \right) \cdot \left(1 + \left(\frac{b+z_2^{-1}}{1+bz_2^{-1}} \right) \right) \quad (3) \end{aligned}$$

With the application of such DST, the perfect reconstruction property of the resulting 2-D filter bank is guaranteed in addition to all wavelet conditions. That because the DST maintains an approximate linear phase processing property, if the reference 1-D digital filter possesses such property [18] (the reference filter is a 1-D Haar filter which is of the linear phase FIR type).

In order to produce the 2-D stable and circular symmetrical filter, the absolute values of a and b must be less than one [17]. In this paper, the values of a and b is chosen to be 0.5.

Let

$$A(z_1^{-1}) = \left(\frac{a+z_1^{-1}}{1+a z_1^{-1}} \right) \quad (4a)$$

and

$$B(z_2^{-1}) = \left(\frac{b+z_2^{-1}}{1+b z_2^{-1}} \right) \quad (4b)$$

Using $A(z_1^{-1})$ and $B(z_2^{-1})$ functions of (4 a & b), $H_0(z_1, z_2)$ can be reduced to

$$\begin{aligned} H_0(z_1, z_2) &= \frac{1}{4} (1 + A(z_1^{-1})B(z_2^{-1})) \\ &\cdot \left(1 + \frac{A(z_1^{-1})}{B(z_2^{-1})} \right) \cdot (1 + A(z_1^{-1})) \cdot (1 + B(z_2^{-1})) \\ &= \frac{1}{4} \left(1 + \frac{A(z_1^{-1})}{B(z_2^{-1})} + A(z_1^{-1})B(z_2^{-1}) + A(z_1^{-1})^2 \right) \\ &\cdot (1 + A(z_1^{-1}) + B(z_2^{-1}) + A(z_1^{-1})B(z_2^{-1})) \\ H_0(z_1, z_2) &= \\ &\frac{1}{4} \left((1 + A(z_1^{-1})^2) + A(z_1^{-1}) \left(B(z_2^{-1}) + \right. \right. \\ &\left. \left. 1Bz_2^{-1} - 1.1 + Az_1^{-1} - 1Bz_2^{-1} + Az_1^{-1} - 1 + Bz_2^{-1} - 1 \right) \right) \end{aligned} \quad (5)$$

The block diagram of 2-D low-pass filter depending on (5) is shown in Fig.1.

The 1-D high-pass filter can also be treated as follows:

$$H_1(z) = \frac{1}{\sqrt{2}} - \frac{1}{\sqrt{2}} z^{-1} \quad (6)$$

The designed 2-D high-pass filter in analysis stage can be formulated as

$$\begin{aligned} H_1(z_1, z_2) &= \\ &\frac{1}{\sqrt{2}} \left(1 - \left(\frac{a+z_1^{-1}}{1+a z_1^{-1}} \right) \left(\frac{b+z_2^{-1}}{1+b z_2^{-1}} \right) \right) \cdot \frac{1}{\sqrt{2}} \left(1 - \right. \\ &\left. \frac{a+z_1^{-1}-11+a}{z_1^{-1}-1b+z_2^{-1}+bz_2} \right) \\ &\frac{1}{\sqrt{2}} \left(1 - \left(\frac{a+z_1^{-1}}{1+a z_1^{-1}} \right) \right) \cdot \frac{1}{\sqrt{2}} \left(1 - \left(\frac{b+z_2^{-1}}{1+b z_2^{-1}} \right) \right) \end{aligned} \quad (7)$$

Using $A(z_1^{-1})$ and $B(z_2^{-1})$ functions of (4 a & b), $H_1(z_1, z_2)$ can be reduced to

$$\begin{aligned} H_1(z_1, z_2) &= \frac{1}{4} (1 - A(z_1^{-1})B(z_2^{-1})) \\ &\cdot \left(1 - \frac{A(z_1^{-1})}{B(z_2^{-1})} \right) \cdot (1 - A(z_1^{-1})) \cdot (1 - B(z_2^{-1})) \\ &= \frac{1}{4} \left(1 - \frac{A(z_1^{-1})}{B(z_2^{-1})} - A(z_1^{-1})B(z_2^{-1}) + A(z_1^{-1})^2 \right) \\ &\cdot (1 - A(z_1^{-1}) - B(z_2^{-1}) + A(z_1^{-1})B(z_2^{-1})) \\ H_1(z_1, z_2) &= \\ &\frac{1}{4} \left((1 + A(z_1^{-1})^2) - A(z_1^{-1}) \left(B(z_2^{-1}) + \right. \right. \\ &\left. \left. 1Bz_2^{-1} - 1.1 + Az_1^{-1} - 1Bz_2^{-1} - Az_1^{-1} + Bz_2^{-1} - 1 \right) \right) \end{aligned} \quad (8)$$

The same block diagram of Fig. 1 can be used to realize the designed 2-D high-pass filter $H_1(z_1, z_2)$ by substituting a subtractor instead of each of the colored

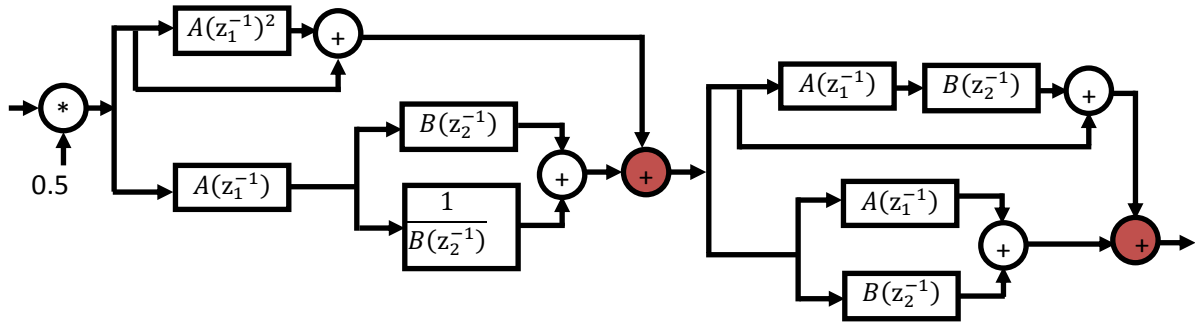


Fig.1 The block diagram of 2-D low-pass filter with all-pass structures.

adders. The 1-D synthesis filter equations can be determined from the corresponding analysis equations as

$$\begin{aligned} F_0(z) &= H_1(-z) = \frac{1}{\sqrt{2}}(1 - (-z)^{-1}) \\ &= \frac{1}{\sqrt{2}}(1 + z^{-1}) = H_0(z) \end{aligned} \quad (9)$$

$$\begin{aligned} F_1(z) &= -H_0(-z) = -\frac{1}{\sqrt{2}}(1 + (-z)^{-1}) \\ &= -\frac{1}{\sqrt{2}}(1 - z^{-1}) = -H_1(z) \end{aligned} \quad (10)$$

From (9) and (10), the 2-D version of such synthesis filters can easily be designed and realized with the same structure.

3.1 The lattice structure

The conventional 1-D discrete wavelet transform architecture produces the approximation and detail coefficients by the use of the convolution function between the input signal and the coefficients of the filter. As known earlier the approximation coefficients are generated by performing the convolution function between the input signal and the coefficients of low-pass filter with a down sampling by two. The detail

coefficients are also generated by performing the convolution function between the same input signal and the coefficients of high-pass filter with the same down sampling. The classical 2-D discrete wavelet transform is performed by applying the 1-D discrete wavelet transform on each row of the 2-D input data and then implementing the same 1-D discrete wavelet transform in each column of the resulting 2-D data.

In this paper, a new 2-D discrete circular Haar wavelet transform is designed and realized as a filter bank using the lattice structure of the two all-pass sections $A(z_1^{-1})$ and $B(z_2^{-1})$. The programmable lattice structure of 2-D low/high pass filter can be extended as a regular unit in the overall system design. Hence, the implementation of the forward 2-D lattice structure is straightforward, as shown in Fig. 2. The 1st stage is applied on each row of the scaled 2-D input data, while the 2nd stage is represented by lattice structure and 2-1 MUX and the 3rd stage is applied on each

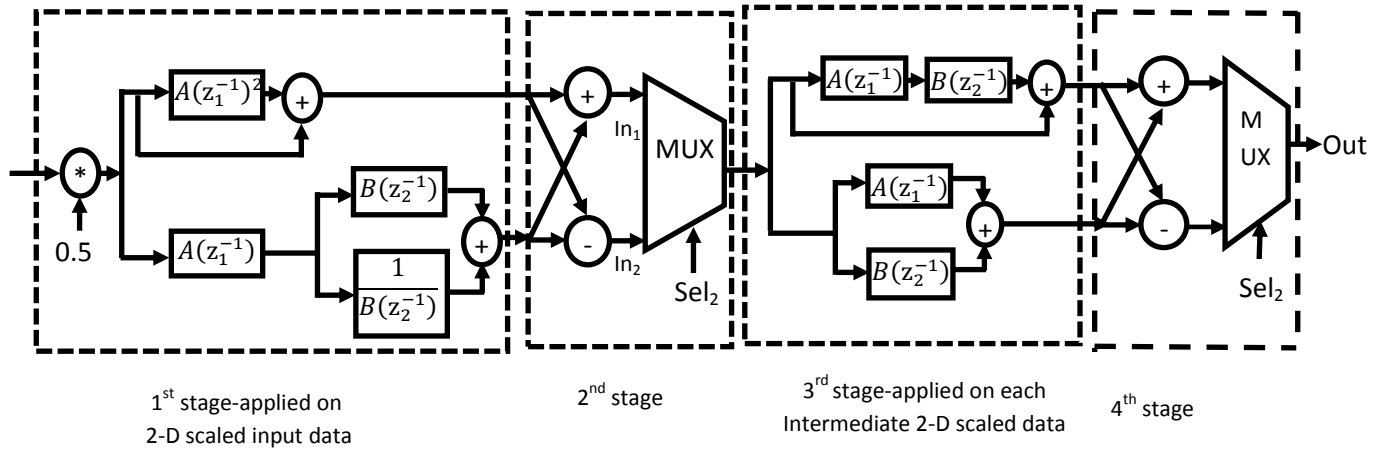


Fig. 2 Lattice structure of 2-D low/high pass analysis filter.

of the intermediate 2-D data. The 4th stage stands for lattice implementation only.

In Fig. 2, Sel₂ determines whether the structure is operating as low or high pass 2-D filter. If Sel₂=0, the structure will operate as 2-D low-pass filter and In₁ is applied as the input to the third stage, while Out will represent the circular low coefficients. If Sel₂ = 1, the structure will operate as 2-D high-pass filter and In₂ is applied as the input to the third stage, while Out will represent the circular high coefficient. The synthesis stage can also be implemented using the same structure with an ending inverter on Out₂ (see Fig. 3) depending on (9) and (10).

3.2 Analysis and synthesis structures

It is clear that the functional block diagrams of the proposed analysis and Synthesis 2-D filters differ only by the kind the input data supplied to the

first stage of the architecture. It is possible to build an integrated structure that can function as multi-level analysis or synthesis 2-D filter architecture by adding multiplexers with a control signal. The block diagram of the programmed 2-D analysis/synthesis lattice filter bank architecture is shown in Fig. 3. In Fig.3 the lattice structure and multiplexer are represented by adder/subtractor blocks. The operation of the lattice structure depends on Sel₃, Sel₂ and Sel₁ as shown in Table 2.

3.3 A multiplier-less 2-D circular wavelet filter bank

To accomplish the design of the proposed 2-D architecture, the parameters a and b are chosen equal to 0.5 to satisfy the stability purposes and approximate linear phase processing with an approximate 2-D circular filter cutoff contour [18]. Thus, the resulting lattice structure of the 2-D circular wavelet

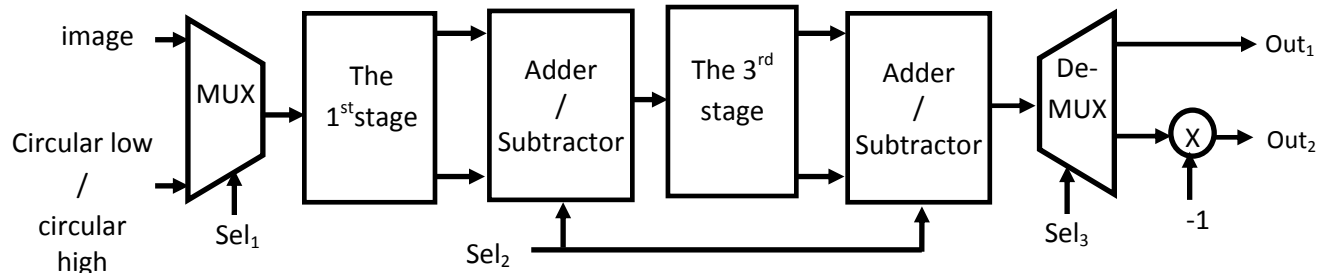


Fig.3 Block diagram of the programmed 2-D analysis/synthesis lattice filter bank architecture.

Table 2. setting the control signals for analysis and synthesis lattice structure.

Sel ₁	Sel ₂	Sel ₃	The input data	The operation	The output data
0	0	0	A pixel of an input image	Low pass analysis filtering	Out ₁ = circular low coefficient Out ₂ = 'X'
0	1	0	A pixel of an input image	High pass analysis filtering	Out ₁ = circular high coefficient Out ₂ = 'X'
1	0	0	LL, LH coefficients	Low pass synthesis filtering	Out ₁ = Reconstructed data Out ₂ = 'X'
1	1	1	HH, HL coefficients	High pass synthesis filtering	Out ₁ = 'X' Out ₂ = Reconstructed data

filter bank can be implemented as multiplier-less and separable sections. Initially, the transfer function of each block in the lattice structure of Fig. 2 can be written as

$$[A(z_1^{-1})]^2 = \left(\frac{a + z_1^{-1}}{1 + a z_1^{-1}} \right) \left(\frac{a + z_1^{-1}}{1 + a z_1^{-1}} \right) = \left(\frac{a^2 + 2a z_1^{-1} + z_1^{-2}}{1 + 2a z_1^{-1} + a^2 z_1^{-2}} \right)$$

with $a = 0.5$. Then

$$[A(z_1^{-1})]^2 = \frac{0.25 + z_1^{-1} + z_1^{-2}}{1 + z_1^{-1} + 0.25 z_1^{-2}} \quad (11)$$

So, that the output function of the block $[A(z_1^{-1})]^2$ which is shown in Fig. 4, can be written as

$$\frac{\text{int}_1(z_1^{-1})}{\text{Image}(z_1^{-1})} = \frac{0.25 + z_1^{-1} + z_1^{-2}}{1 + z_1^{-1} + 0.25 z_1^{-2}}$$

$$\begin{aligned} \text{int}_1(z_1^{-1}) \cdot (1 + z_1^{-1} + 0.25 z_1^{-2}) \\ = \text{Image}(z_1^{-1}) \cdot (0.25 + z_1^{-1} + z_1^{-2}) \end{aligned}$$

$$\begin{aligned} \therefore \text{int}_1(n_1) &= 0.25 * \text{Image}(n_1) \\ &+ \text{Image}(n_1 - 1) + \text{Image}(n_1 - 2) \\ &- \text{int}_1(n_1 - 1) - 0.25 * \text{int}_1(n_1 - 2) \end{aligned} \quad (12)$$

The functional block $[A(z_1^{-1})]^2$ can be implemented in a shift and add multiplier-less structure. Such structure is a summation of the input signal and the feedback of the output signal without multipliers as shown in Fig. 4.

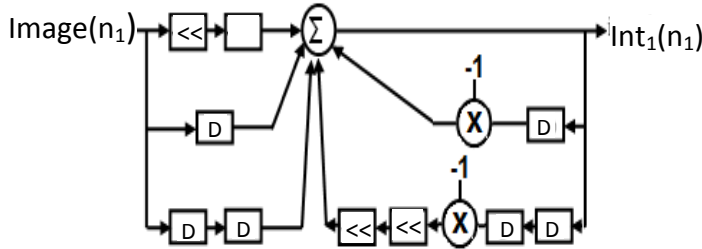


Fig. 4 Shift and add multiplier-less block diagram of $[A(z_1^{-1})]^2$. D is a delay unite and \ll is a single- digit shift.

On the other hand, the block of $A(z_1^{-1})$ can be implemented as a multiplier-less function as follows:

$$A(z_1^{-1}) = \left(\frac{a + z_1^{-1}}{1 + a z_1^{-1}} \right)$$

$$\frac{\text{int}_2(z_1^{-1})}{\text{Image}(z_1^{-1})} = \frac{0.5 + z_1^{-1}}{1 + 0.5z_1^{-1}}$$

$$\begin{aligned} \text{int}_2(z_1^{-1}) * (1 + 0.5z_1^{-1}) \\ = \text{Image}(z_1^{-1}) * (0.5 + z_1^{-1}) \end{aligned}$$

$$\therefore \text{int}_2(n_1) = 0.5 * \text{Image}(n_1) + \text{Image}(n_1 - 1) - 0.5 * \text{int}_2(n_1 - 1) \quad (13)$$

The shift and add block diagram of $A(z_1^{-1})$ without multipliers is shown in Fig. 5. The processing in Fig. 5 is held on raw-based algorithms.

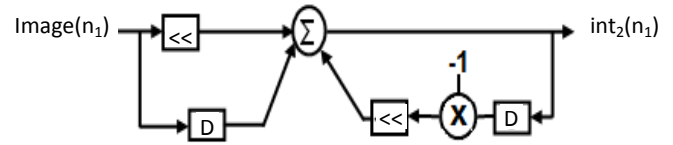


Fig. 5 Shift and add multiplier-less block diagram of $A(z_1^{-1})$.

Similarly, the transfer function of $B(z_2^{-1})$ can be written as

$$B(z_2^{-1}) = \left(\frac{b + z_2^{-1}}{1 + bz_2^{-1}} \right)$$

$$\frac{\text{Out_data}_2(z_2^{-1})}{\text{In_data}_1(z_2^{-1})} = \frac{0.5 + z_2^{-1}}{1 + 0.5z_2^{-1}}$$

where

Out_data₂(z₂⁻¹) is resulting output data.

In_data₁(z₂⁻¹) is intermediate resulted input data.

$$\begin{aligned} \therefore \text{Out_data}_2(n_2) &= 0.5 * \text{In_data}_1(n_2) + \\ &\text{In_data}_1(n_2 - 1) - 0.5 * \text{Out_data}_2(n_2 - 1) \end{aligned} \quad (14)$$

The multiplier-less block diagram for $B(z_1^{-1})$ is similar to the block diagram of Fig. 5, with input Image (n₁) and output int₂ being replaced by input In_data₁ (n₂) and output Out_data₂(n₂), respectively. In such case, the processing will be held on column-based algorithms.

4. FPGA Implementations

At the beginning, every pixel of the input image is shifted right by one digit to apply the multiplication operation by 0.5 as shown in Fig. 2, Then the two blocks, *i.e.*, the block of $(1 + A(z_1^{-1})^2)$ and the block of $A(z_1^{-1})$ begin to read the input data (input image) from block RAM and perform the operation of the two blocks in parallel. The basic cells of the proposed structure are implemented on a Xilinx Spartan-3E. The results are summarized in Table 3.

Table 3. The LUT number of cells and maximum frequency for basic blocks of the proposed structures.

Type of Structure	No. of cells	Maximum Frequency (MHz)
Analysis Structure	300	198.447
Synthesis Structure	420	177.8

5. Performance Evaluation

The Deflection Ratio (DR) is used as an objective assessment parameter to evaluate the performance of the proposed 2-D lattice filter by applying a Matlab 7.2 program. DR is used here as a performance estimator. A proposed formula for this deflection is given by [19], [20]

$$DR = \frac{1}{R \times C} \sum_{r,c} \left(\frac{I_c(r,c) - MV}{SD} \right) \quad (15)$$

where

$$MV = \frac{\sum_{r,c} I_c(r,c)}{R \times C}, \quad (16)$$

$$SD = \sqrt{V} \quad (17)$$

and

$$V = \frac{\sum_{r,c} [I_c(r,c) - MV]^2}{R \times C} \quad (18)$$

$I_c(r,c)$ is the coefficient image, MV is the mean value, V is the variance and SD is the standard deviation.

The ratio DR should be higher at pixels with stronger reflector points and lower elsewhere. As shown in Table 4, different images (Camera man, Lena, Barbara, Peppers) are used to compare the values of deflection ratio between the resulting coefficients of the proposed 2-D lattice circular filter design and classical filter design. The Matlab results of deflection ratio calculated from the designed 2-D lattice filter are better than those of the classical 2-D Haar design especially at the edges that appear in the LH, HL and HH sub-band images.

The correlation factors (CFs) between the input and reconstructed images for both classical and proposed designs are also calculated and listed in Table 4. It can be seen that, CF values are better in the proposed design.

Table 4- Objective assessment parameters of the proposed design and the classical design.

Images 256x256	Objective Assessment Parameters				
	Classical 2-D Haar Design			The Proposed Design	
	DR		CF	DR	CF
	DR of LH,HL and HH	Average of DR in LH,HL,HH			
Camera man	LH= -3.69×10^{-17}	-1.89×10^{-17}	0.8925	1.45×10^{-17}	0.902
	HL= -1.36×10^{-17}				
	HH= -4.5×10^{-18}				
Lena	LH= -2.78×10^{-18}	1.5×10^{-17}	0.89	8.45×10^{-17}	0.903
	HL= 4×10^{-17}				
	HH= -8.9×10^{-18}				
Peppers	LH= 1.6×10^{-17}	5.9×10^{-18}	0.9046	-7×10^{-18}	0.926
	HL= 0				
	HH= -1.8×10^{-18}				
Barbara	LH= -5.3×10^{-18}	-8.4×10^{-18}	0.9004	-2.65×10^{-17}	0.91
	HL= -6.8×10^{-18}				
	HH= -1.3×10^{-17}				

6. Conclusions

In this paper, a new and effective algorithm for 2-D circular-support wavelet transform circular proposed. The method has used a 1st order 1-D all-pass sections in a lattice filter structure to build the final 2-D discrete wavelet transform architecture. The design has been based on a single programmable structure, which can be integrated to form separable 2-D all-pass filter in both directions (horizontal and vertical). These separable structures have been connected

with each other on a single programmable integrated architecture that can function as a single forward or backward circular 2-D discrete wavelet transform. Such connection highlights the simplicity, regularity and modularity properties of the proposed system. In addition, A pipeline technique has been used to increase the speed of computation in the proposed architecture. It has been shown that the 2-D circular-support decomposition scheme can effectively improve the operation of extracting both

approximation and detail coefficients from the original images based on 2-D circular filters instead of using the traditional two-stage 1-D filter decomposition in classical 2-D discrete wavelet transform.

References

- [1] M. A. Mirzaei, "Acceleration of Face Detection Algorithm on an FPGA", M. Sc. Thesis in Vision and Robotics (VIBOT), University Centre Condorcet, University of Bourgogne, France, Group of Circuit and Systems, Department of Electronics Engineering, June 2011.
- [2] A. Schreiner, "Image Processing Techniques for Face Recognition" University of Wisconsin Madison- ECE 533 Project, 2006.
- [3] K. H. Talukder, K. Harada, "Haar Wavelet Based Approach for Image Compression and Quality Assessment of Compressed Image", IAENG International Journal of Applied Mathematics- IJAM, Vol. 36, No. 1, 2007.
- [4] C. Xiong, J. Tian, and J. Liu, "Efficient Architectures for Two-Dimensional Discrete Wavelet Transform using Lifting Scheme", IEEE Transactions on Image Processing, Vol. 16, No. 3, pp. 607 – 614, March 2007.
- [5] C. Cheng, and K. K. Parhi, "High-Speed VLSI Implementation of 2-D Discrete Wavelet Transform," IEEE Transactions on Signal Processing, Vol. 56, No. 1, pp. 393- 403, Jan. 2008.
- [6] J. M. Abdul-Jabbar and Z. N. Abdulkader, "Iris Recognition using 2-D Elliptical-Support Wavelet Filter Bank", International Conference on Image Processing Theory, Tool and Applications- IPTA 2012, Istanbul, Turkey, 15-18 Oct., pp. 359 – 363, 2012.
- [7] J. M. Abdul-Jabbar and H. N. Fathee, "Design and Realization of Circular Contourlet Transform", Al-Rafidain Engineering Journal, Vol. 18, No. 4, pp. 28 - 42, Aug. 2010.
- [8] M. Vishwanath, R. M. Owens, and M. J. Irwin, "VLSI Architectures for The Discrete Wavelet Transform", IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 42, No. 5, pp. 305–316, May 1995.
- [9] Chao-T. Huang, Po-C. Tseng, and Liang-G. Chen, "Analysis and VLSI Architecture for 1-D and 2-D Discrete Wavelet Transform", IEEE Transactions on Signal Processing, Vol. 53, No. 4, pp. 1575-1586, April 2005.
- [10] B. K. Mohanty, A. Mahajan and P. K. Meher, "Area and Power- Efficient Architecture for High-Throughput Implementation of Lifting 2-D DWT" IEEE Transactions on Circuits and Systems-II, express brief , May 2012.
- [11] D. Sowjanya, K. N. H. Srinivas and P. Venkata Ganapathi, "FPGA Implementation Of Efficient VLSI

Architecture for Fixed Point 1-D DWT using Lifting Scheme” in VLSI International Journal of VLSI Design & Communication Systems (VLSICS) Vol. 3, No. 4, pp. 37-48, Aug. 2012.

[12] T. C. Denk and K. K. Parhi , “ VLSI Architectures for Lattice Structure Based Orthonormal Discrete Wavelet Transforms”, IEEE Transactions on Circuits And Systems-II: Analog and Digital Signal Processing, Vol. 44, No. 2, pp. 129-132, Feb. 1997.

[13] M. N. Kumar, J. Hemanth and K. D. Prasad, “VLSI Implementation of DWT Using Systolic Array Architecture”, International Journal of Recent Technology and Engineering (IJRTE), Vol. 1, Issue-4, pp. 67-73, Oct. 2012.

[14] J. Fridman and E. Manolakos, “Distributed Memory and Control VLSI Architectures for The 1-D Discrete Wavelet Transform,” in VLSI Signal Processing, VII, pp. 388–397, 1994.

[15] R. Jain and P. R. Panda, “Memory Architecture Exploration for Power-Efficient 2D-Discrete Wavelet Transform” IEEE Conference Proceedings: 20th VLSI Design - 6th Embedded Systems, pp. 813 – 818, Jan. 2007.

[16] M. I. Mahmoud, M. I. M. Dessouky, S. Deyab, and F. H. Elfouly, “Comparison between Haar and Daubechies Wavelet Transformations on FPGA Technology”, World Academy of

Science, Engineering and Technology, Vol. 26, pp. 68-72, 2007.

[17] S. Alseyab, O. A. Al Heyasat and J. M. Abdul-Jabbar, “Design of 2-D IIR filter with linear phase using modified digital spectral transformation” Alexandria Engineering Journal, Faculty of Engineering Alexandria University, Egypt, Vol. 44, No. 6, pp. 865-881, 2005.

[18] B. A. Shenoi and P. Misra, “Design of Two-Dimensional IIR Digital Filter with Linear Phase,” IEEE Trans. Circuits Syst.– II: Analog and Digital Signal Process., Vol. 42 (2), pp. 124-129, 1995.

[19] M. Mastriani, A. E. Giraldez, "Smoothing of Coefficients in Wavelet Domain for Speckle Reduction in Synthetic Aperture Radar Images", The International Congress for Global Science and Technology (ICGST), International Journal on Graphics, Vision and Image Processing (GVIP), GVIP, Special Issue on Denoising, pp.1-8, 2007. www.icgst.com

[20] M. Mastriani and A. E. Giraldez, "Kalman's Shrinkage for Wavelet-Based De-speckling of SAR Images", International Journal Of Intelligent Technology, Vol. 1, No. 3, pp. 190-196, 2006.