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Digital Single Phase Power Factor Optimizer Based on FPGA

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ABSTRACT

In this paper, an FPGA (Field-programmable gate array) model of digital single phase power factor optimizer has been built. The proposed optimizer is based on measuring the phase shift time between voltage and current waveforms. Therefore, it is required to reduce this time to make the voltage and current waves in phase as possible. Thus, the power factor will be in maximum value (closed to unity). The process of improving the power factor is carried out by connecting a set of capacitors in parallel with the load. The proposed power factor optimizer has been built using VHDL (Very high speed integrated circuit Hardware Description Language), simulated using Xilinx ISE 9.2i package and implemented using Spartan-3A XC3S700A FPGA kit. Implementation and Simulation behavioral model results show that the proposed optimizer satisfies the specified operational requirements and reflected impressive results when applied to different loads.

Keywords: Digital Power Factor Optimizer, Power Factor Correction, Single Phase Power Factor Optimizer, FPGA.

اعتماد مصفوفة البوابات القابلة للبرمجة موقعياً في محسن معامل القدرة الرقمي ذو الطور الواحد

الخلاصة

تم بناء نموذج FPGA (لمصفوفة البوابات القابلة للبرمجة موقعياً) لمحسن معامل القدرة الرقمي ذو الطور الواحد. يعمل محسن معامل القدرة الذي على أساس قياس فرق زمن الطور بين موجتي الفولتية والتيار. بعد ذلك يقوم بتقليل هذا الزمن لجعل موجتي الفولتية والتيار في نفس الطور. بالتالي فان قيمة معامل القدرة سوف تصل إلى أعظم قيمة (قريب من الواحد). ان عملية تحسين معامل القدرة تتم من خلال ربط مجموعه من المتسعات على التوازي مع الحمل. تم بناء محسن معامل القدرة المقترح باستخدام لغة الـ VHDL (لغة توصيف العتاد للدارات المتكاملة ذات السرعات المرتفعة جدا) وتمت محاكاته باستخدام Xilinx ISE 9.2i package وتم تنفيذه باستخدام Spartan-3A XC3S700A FPGA kit. لقد أظهرت نتائج تنفيذ و محاكاة هذا النموذج بان المحسن المقترح قد حقق المتطلبات التشغيلية المحددة واظهر نتائج مبهرة حين طبق على أحمال مختلفة.

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INTRODUCTION

The people necessity makes them seek for a solution; so it is required to think how to find solutions to reduce the cost of consuming electrical energy, since the electricity is a great need for each person on the earth. This led to find a solution to reduce power consumption, which is done by improving the power factor. Improving the power factor will reduce the amount of electrical power. When this happens, it is possible to imagine the vast amount of energy saved in the world.

Power factor (PF) is defined as the ratio of real power to apparent power, where real power produces real work and apparent power is the total power that a power company has to supply [1]. When PF is not 100%, the current waveform does not follow the voltage waveform. This results in power losses and may also cause harmonics that travel down the neutral line and disrupt other devices connected to the line [1, 2]. The power-factor-correction (PFC) circuit basically shapes the input current waveform to be the replica of the input voltage waveform and exactly in phase with it [3].

Low power factor in the power distribution system causes the energy crisis in the supply of energy resources. Most of industrial electric loads have a low power factor not exceeding 0.8 and thus contributes to the distribution system losses [2, 4]. There are different methods of power factor correction (optimizer) implemented with large lagging or leading nonlinear loads [5].

There are various types of single phase PFC converters [6]. Traditionally, the analog control model is the first choice for designing the system for PFC, known as analog-PFC. There are many integrated circuits available for analog-PFC. It is simple and fast to implement because the control algorithm and the performances of the system are predefined by the manufacturer [7]. On the other hand analog-PFC systems have some strong drawbacks. High part count, susceptibility to aging and environment variations, along with the fixed control algorithm, are making them less attractive for new designs of PFC systems [8].

The usage and performance of Field programming gate arrays (FPGA) have risen significantly in recent years for its reconfigurability and flexibility. The FPGA has been applied to analyzing and controlling a power system [9-10]. The major difference between FPGA and DSP-based solutions is that FPGA enables simultaneous execution of all control subroutines, which allows high performance and novel control methods [11].

The FPGAs are two-dimensional arrays of logic blocks and flip-flops with an electrically programmable interconnection between logic blocks. The interconnections consist of electrically programmable switches which is the cause of that FPGA differs from custom ICs, as custom IC is programmed using integrated circuit fabrication technology to form metal interconnections between logic blocks. The ability to reconfigure functionality to be implemented on a chip gives a unique advantage to designer to carry out his system on an FPGA. It reduces the time to market and significantly reduces the cost of production [12].

The purpose of this paper is introducing a proposed approach of a digital single phase power factor optimizer based on FPGA. This optimizer is improving the value of the power factor by measuring the duration time between voltage and electric current waveforms. Accordingly, adding the capacitive load sequentially to

reduce the shift time between them in order to make the power factor close to unity.

THE PROPOSED DIGITAL OPTIMIZER

The proposed power factor optimizer (PFO) operates depending on measuring the phase shift time between the voltage and current waveforms. This time represents the phase angle between them. According to equation (1) in [1], when the value of this angle is small, the power factor will be close to the optimum value which is equal to one.

$$PF = \cos q \quad \text{.....(1).}$$

where q :is the phase angle between the voltage and the current waveforms.

The proposed optimizer makes the voltage waveform in phase with current waveform by connecting a set of parallel capacitors with the load. These capacitors will reduce the time shift between the voltage and current. The process of adding capacitors is performed sequentially, with the optimizer adding one capacitor per unit time. Thereafter, measures the angle between the voltage and current at each unit time until the power factor reached the optimal value.

Figure (1) shows the block diagram of the proposed digital PFO. As illustrated in this diagram, the voltage and current must be converted to square wave, so they will be compatible with FPGA integrated circuit.

The pins' assignment of the digital PFO is illustrated in Figure (2). The current wave entered to the PFO via (Iin) pin while (Vin) pin is used for voltage wave. The optimizer connects the capacitors to the load via the switches assigned by (S0-S9). The value of the phase shift angle will be displayed on (PA) pins.

FPGA MODEL OF THE PROPOSED PFO

The FPGA model of a digital single phase power factor optimizer is built using VHDL (Very high speed Hardware Description Language), and implemented and simulated using Xilinx ISE 9.2i package. This model consists of two parts, entity declaration and process. The entity declaration part, shown in Figure (3), is used to declare the signals of the digital power factor optimizer. The process part will be responsible for the evaluating the phase shift time between the voltage and current waves, connecting parallel capacitors to the load out of switches (S0-S9) to force the power factor reach to unity as possible, and display the value of the phase shaft angle between the voltage and current. The process part flowchart of the digital power factor optimizer is illustrated in Figure (4).

The simulation behavioral model test results of the digital PFO are shown in Figures (5-7). As demonstrated in Figure (5) when the voltage and current be in phase the switches are off (no capacitor is connected). If the phase angle is greater than the desired value, the PFO will connect the parallel capacitor sequentially, as it is clear in Figure (6) and Figure (7).

Figure (8) shows the Register Transfer Level (RTL) schematics for PFO when the FPGA model is implemented using Xilinx ISE 9.2i package. The RTL is basic

level for FPGA design entry, which represent a digital circuit as a set of connected primitives (adders, counter, multiplexers, registers etc.).

The results displayed in Figures (9-11) are appeared when the power factor optimizer is tested at 10 amperes current and variable load. As explained from the previous figures, the power factor for each case is closed to unity; the current reduction reaches 70% of its maximum value according to the load, so the power is reduced to the same percentage. Furthermore, the phase shift angle is decreased to contact the lowest value. Figures (9-11) are plotted using MATLAB according to the results found from the PFO testing.

Implementation of the proposed system is illustrated in Figure (12); a variable resister and variable inductance are employed as variable load as shown in Figure (12-a). Figure (12-b) shows the comparator circuit that covert the input voltage and current signal to square wave. The square waves are received by the Spartan-3A XC3S700A FPGA kit. The FPGA kit operates as a controller which calculates the duration difference time between the two square wave signals, obtain the phase angle between them and send signals to connect the shunt capacitors as cleared in Figure (12-c). The shunt capacitors are connected to the circuit through a set of relays to improve the power factor as shown in Figure (12-d). As illustrated in Figure (12-e) there is a phase shift between the voltage signal and current signal. This phase shift is disappeared when the PFO circuit shown in Figure (12-f) is employed to make it as illustrate in Figure (12-g).

CONCLUSIONS

Traditional analog power factor correction (optimizer) are not effective and not accurate in comparison with the digital PFO, This is due to the fact that the analog PFC depends on the fixed control algorithm, involves several disadvantages, high part count, and susceptibility to aging and environment variations. Subsequently, the digital PFO is more powerful and appropriate to model.

In this paper, the FPGA model of a proposed design single phase digital power factor optimizer has been presented. This optimizer is based on measuring the phase shift time between voltage and current. Thus, the value of the phase angle between the voltage and current are available. Through this angle will be calculated the amount of power factor. This PFO improves the power factor by connecting a set of parallel capacitors to the load to perform the PF close to unity.

The proposed PFO is suitable for use in homes, manufactures, factories, and in many other applications to reduce the electrical power consumption and the cost of electricity.

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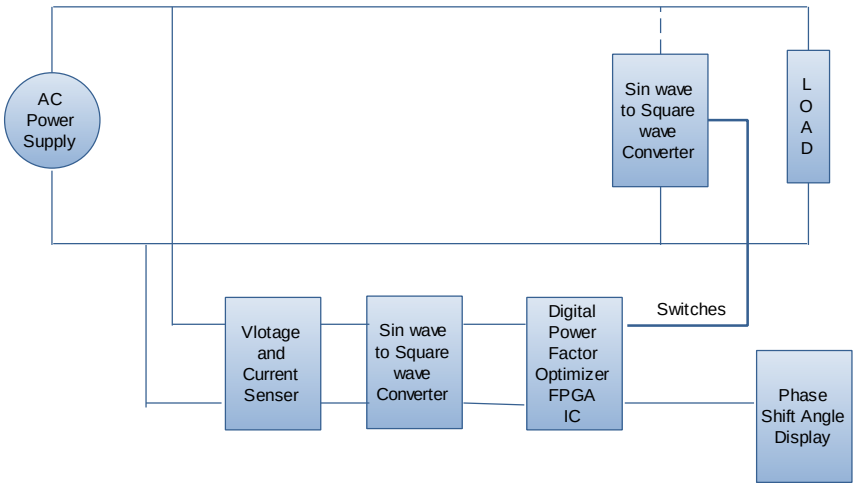


Figure (1): Digital power factor optimizer block diagram.

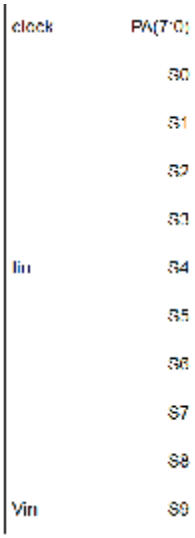


Figure (2): Digital power factor optimizer pins.

```
entity pfc is
port(clock:in std_logic;
Vin:in std_logic;
Iin:in std_logic;
S0:out std_logic;
S1:out std_logic;
S2:out std_logic;
S3:out std_logic;
S4:out std_logic;
S5:out std_logic;
S6:out std_logic;
S7:out std_logic;
S8:out std_logic;
S9:out std_logic;
PA:out std_logic_vector(7 downto 0)
);

end pfc;
```

Figure (3): The entity source code declaration.

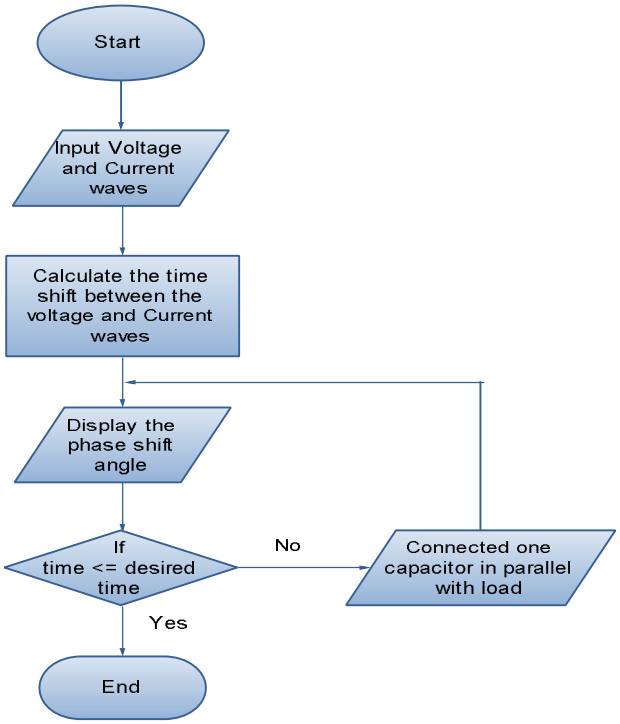


Figure (4): The flowchart of digital power factor optimizer.

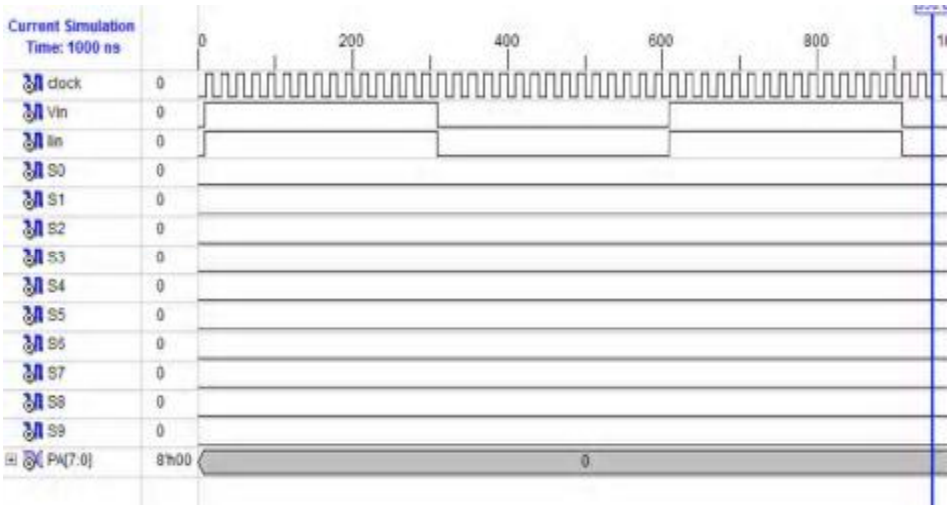


Figure (5): Simulation behavioral model when the voltage in phase with current.

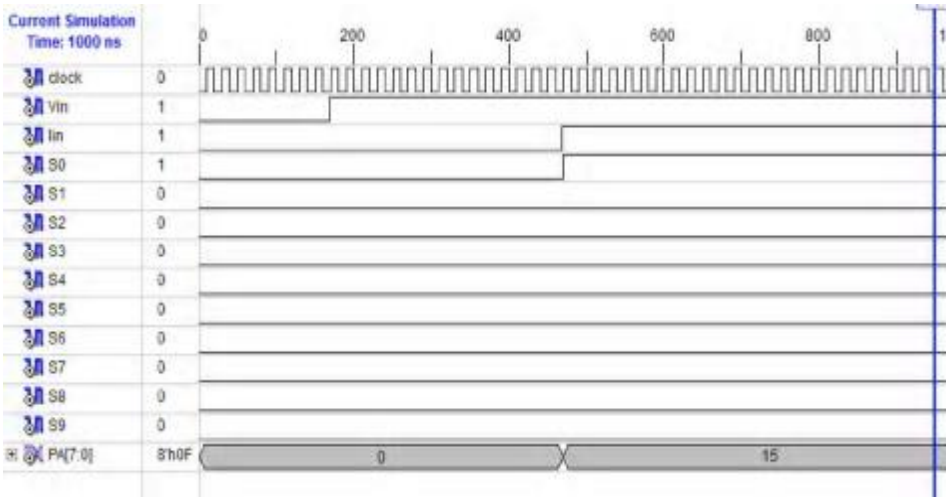


Figure (6): Simulation behavioral model when the phase shift angle greater than desired value (one capacitor is connected).

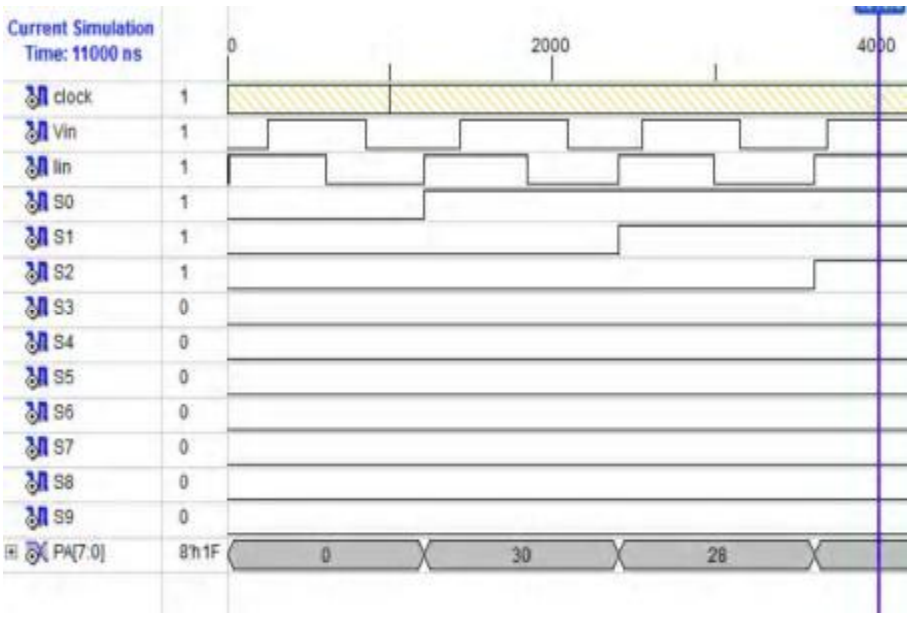


Figure (7): Simulation behavioral model when the phase shift angle greater than desired value (three capacitors are connected).

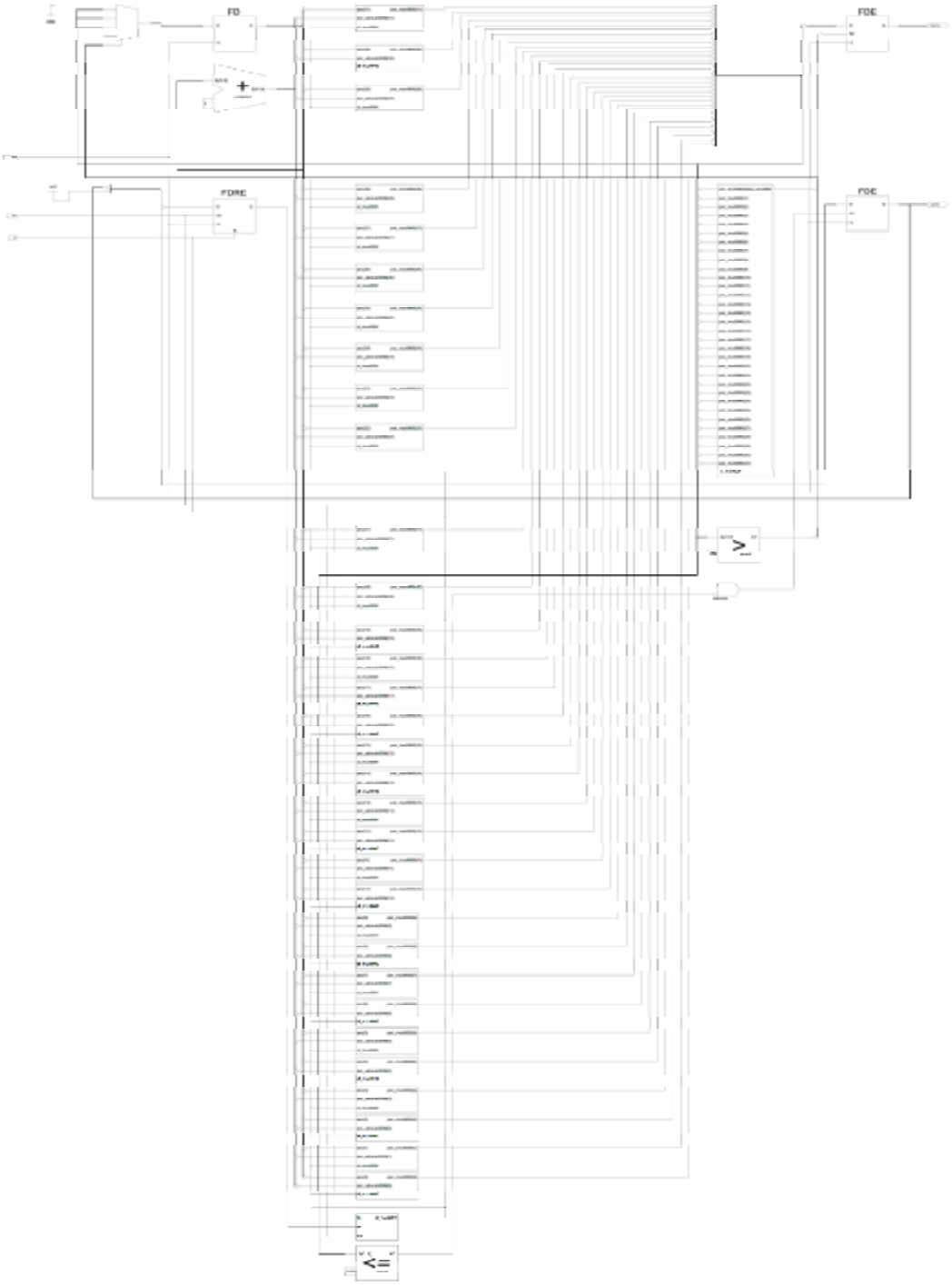


Figure (8): The RTL schematics of digital power factor optimizer.

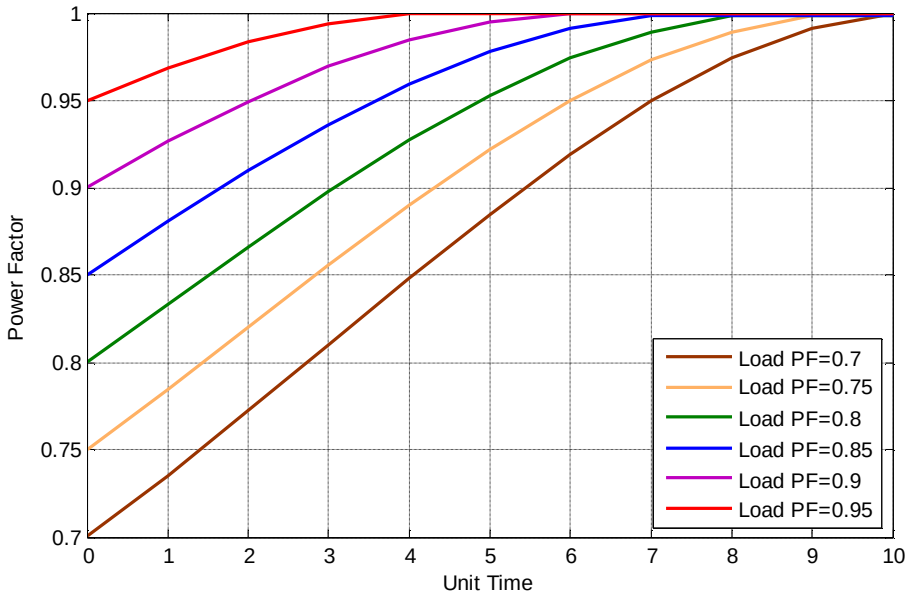


Figure (9): The relationship between the power factor and the time at variable load.

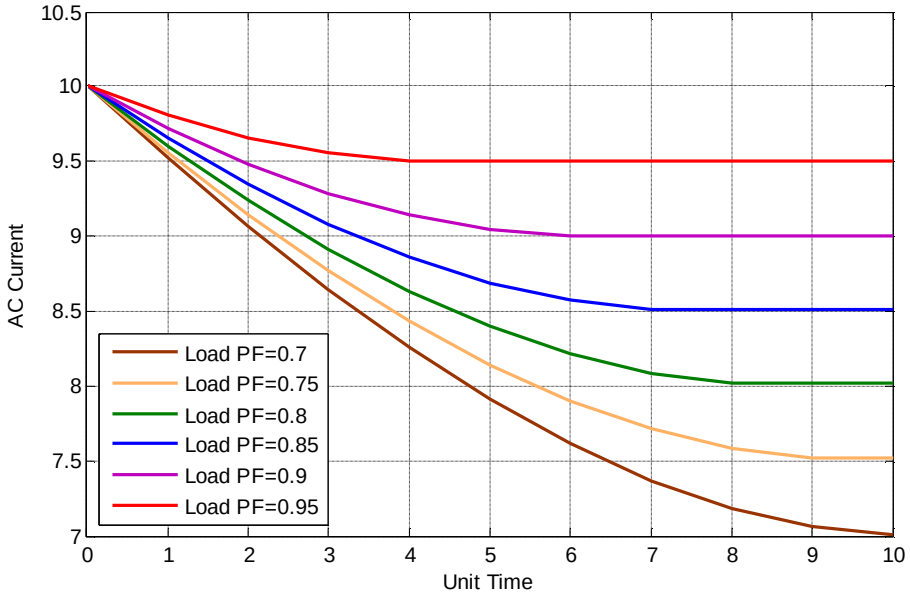


Figure (10): The relationship between the currents and the time at variable load.

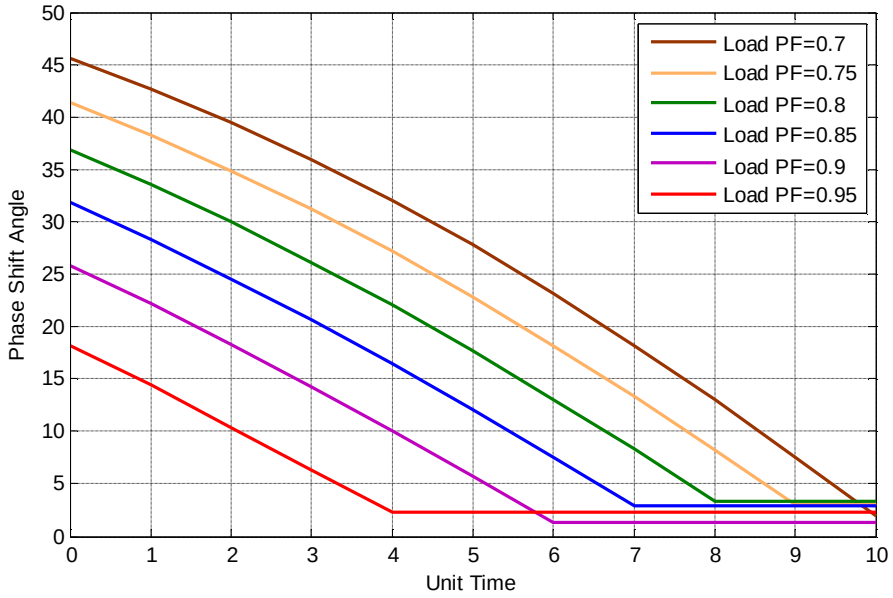
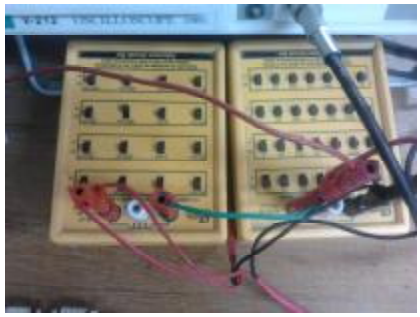
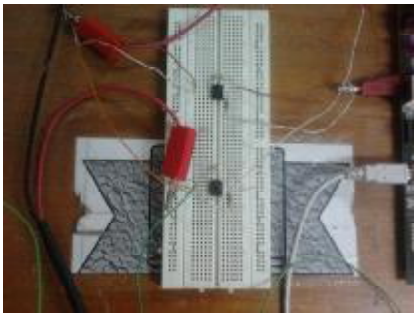


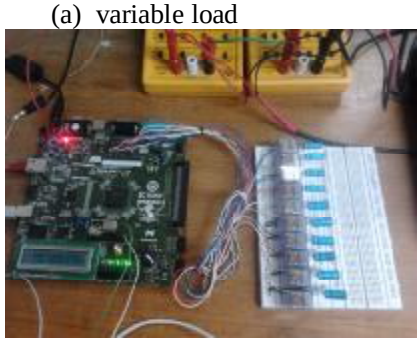
Figure (11): The relationship between the phase shift angle and the time at variable load.



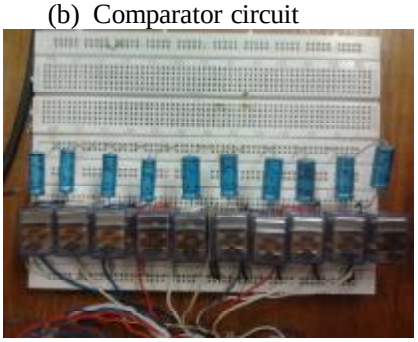
(a) variable load



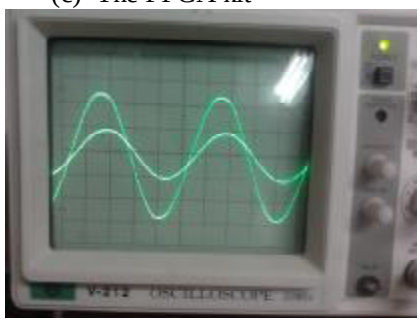
(b) Comparator circuit



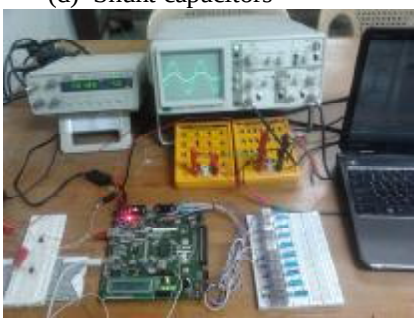
(c) The FPGA kit



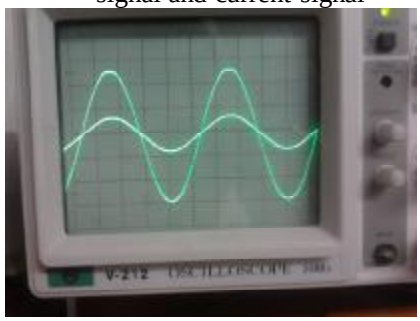
(d) Shunt capacitors



(e) phase shift between the voltage signal and current signal



(f) The PFO circuit



(g) The phase shift disappeared

Figure (12) Implementation of the proposed PFO using the Spartan-3A XC3S700A FPGA kit.