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# A Second-Order Single Loop Oversampling Analog-to-Digital Converter (ADC) with Proposed Hybrid Feedforward/Feedback Architecture

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**ABSTRACT**

This paper proposes hybrid architecture of feedforward/feedback second order single-loop modulator for high resolution analog-to-digital converter (ADC) applications. Different techniques for oversampling modulator are discussed. The proposed architecture consists of three stages. The first stage is $2^{nd}$ order single loop oversampling ADC with novel feedforward/feedback architecture. In the second stage, an error cancellation circuit (ECC) is proposed at the output of the modulator to noise shaping of quantization noise. In addition, the third stage is a decimation filter in order to reduce the oversampling ratio (OSR) which is suitable for broadband applications. With low OSR=24, the signal-to-noise ratio (SNR) is improved about 55 dB if compared with traditional architecture (feedback single-loop high order topology). The achieved resolution or the effective number of bits (ENOB) is (22-bit). With high OSR=256, the net improvement in quantization noise reduction is 64 dB if compared with feedforward architecture (single-loop high order) and the ENOB=28. Finally a 1-bit quantizer is used in the proposed architecture which greatly decreases the circuit implementation complexity and power consumption. Simulation results show the superiority performance of proposed hybrid architecture as compared with traditional modulator topologies (feedforward and feedback).

**Keywords:** ADC, feedforward, feedback, single-loop high order **converter**.

# محول ألاشاره الكمية الى الرقمية عالي العينة من الدرجة الثانية بمعمارية هجينة مقترحة (التغذية الامامية/التغذية العكسية)

**الـــخـــلاصـــة**

يقترح هذا البحث معمارية هجينة لمضمن الاشارة من الدرجة الثانية لتطبيقات محول الاشارة الكمية الى الرقمية عالية الدقة. تم مناقشة عدة تقنيات لمضمن الاشارة عالي العينة. المعماريـــة المقترحة تتكون من ثلاث مراحل. المرحلة الاولى هي محول الاشارة الكمية الى الرقمية مـــن الدرجة الثانية بمعمارية جديدة (Feedforward/Feedback). المرحلة الثانية هي دائرة الغـــاء



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الخطأ المقترحة لتقليل ضوضاء التكمية (Quantization noise) عند محول الاشارة المقترح. أضافة الى ذلك المرحلة الثالثة هي (Decimation filter) لتقليل معدل عالي العينة (OSR) وهو مناسب لتطبيقات الحزمة العريضة. عند OSR منخفض، تم تخفيض ضوضاء التكمية بمقدار ($55\,dB$) اذ ماتم مقارنة مع معمارية التغذية العكسية التقليدية ( Feedback architecture) من نوع(single-loop high order). تم الحصول على دقة عالية تصل الى (22-bit) للنظام المقترح. عند OSR عالي، تم تخفيض ضوضاء التكمية بمقدار ($4\,dB$ 6) اذ ماتم مقارنة مع معمارية التغذية الامامية (Feedforawrd architecture) من نوع (Single-loop high order) وبدقة تصل الى (28-bit). اخيرا تم استخدام ( 1-bit quantizer) في المعمارية المقترحة والتي تخفض من تعقيد بناء الدائرة و من استهلاك الطاقة. اظهرت نتائج المحاكاة أداء متفوقا لمعمارية الهجينة المقترحة عند المقارنة مع (Feedforward and feedback topologies) .

## INTRODUCTION

With the recent developments in both wired and wireless communications, there is a need to analog-to-digital converters (ADCs) at megahertz (MHz) with high resolution at low voltage environments [1]. Conventional ADC architectures (Flash and successive approximation) are not suitable for high resolution applications because of the need to near-ideal analog components and/or precise trimming. To implement a high resolution ADC converter, the oversampling modulator is considered a suitable approach and widely used due to its simplicity and effectiveness [2]. Oversampling ADC or delta-sigma converter, as shown in fig.1 is based on the principle that the input signal is oversampled and the quantization noise is shaped and later removed by digital filters. The oversampling ratio (OSR) is defined as [3]:

$$OSR = \frac{f_S}{f_{Ny}} \qquad (1)$$

Where: $f_S$ = sampling frequency,

$f_{Ny}$ = Nyquist rate.

The in-band quantization noise power ( $N_q^{\,2}$) with oversampling is given by [3]:

$$N_q^{\,2} = \frac{s_q^{\,2}}{f_S}\int_{-f_b}^{f_b} df = \frac{s_q^{\,2}}{OSR} \qquad (2)$$

Where: $f_b$ = signal bandwidth,

$s_q^2$ = the noise power.

Compared to a Nyquist rate converter, the noise power is reduced by OSR. The noise shaping filter of converter distributes the quantization error or noise so as to be very low in the band of interest. By using superposition, the loop output of fig.(1a) is determined as:

$$y(z) = \frac{H(z)}{1+H(z)}.x(z) + \frac{1}{1+H(z)}.q(z) \qquad (3)$$

Where: H (z) = $Z^{-1}/(1-Z^{-1})$ .

Two transfer functions are used to determine ADC performance, a Signal Transfer Function of the system (STF) and a Noise Transfer Function of the system (NTF). These transfer functions are given by [3]:

$$STF(z) = \frac{y(z)}{x(z)}\Big|_{q(z)=0} = \frac{H(z)}{1+H(z)} = Z^{-1} \qquad (4)$$

$$NTF(z) = \frac{x(z)}{q(z)}\Big|_{x(z)=0} = \frac{1}{1+H(z)} = (1-Z^{-1}) \qquad (5)$$

Substituting equations (4) and (5) by equation (3), the loop output is determined as:

$$y(z) = x(z).Z^{-1} + q(z).(1-Z^{-1}) \qquad (6)$$

Where: $x(z)$ is input signal, STF (Signal Transfer Function) = $z^{-1}$, $y(z)$ is output signal and $q(z)$ is quantization noise of the converter, as shown in fig.(1b).

A general NTF (Noise Transfer Function) for high order converter is given by [3]:

$$N_q(z) = (1-z^{-1})^L \times q(z) \qquad (7)$$

Where: L is the converter order.

The ideal SNR of converter is given by [4]:

$$SNR = 10.Log\frac{3}{2}.\frac{(2L+1)}{p^{2L}}.(OSR)^{2L+1} \qquad (8)$$

Where: L is the converter order.

And the resolution bits or the effective number of bits (ENOB) is given by [3]:

$$ENOB = (SNR - 1.76)/6.02 \qquad (9)$$

Increasing the order of the converter improves the performance. In general, for an L-order modulator, the SNR improvement is (6L+3) dB or (L+0.5) bits per doubling the OSR [5].

## OVERSAMPLING CONVERTER TOPOLOGIES

The single-loop high order oversampling converter topology can be divided into two classes: feedback (FB) and feedforward (FF) [3,7].

### Feedback Topology

The feedback architecture, as shown in fig.(2a), is the most commonly used topology of oversampling ADC. The output can be expressed as [6]:

$$y(z) = x(z)z^{-2} + q(z)(1 - z^{-1})^2 \qquad (10)$$

The NTF provides a second-order noise-shaping function for the quantization noise of the converter.

The output signals of the first and second integrators, ($v_1(z)$ and $v_2(z)$), are as follows:

$$v_1(z) = z^{-1}(1 - z^{-1})x(z) - z^{-1}(1 - z^{-1})q(z) \qquad (11)$$

$$v_2(z) = z^{-2}x(z) - z^{-1}(2 - z^{-1})q(z) \qquad (12)$$

From equations (11) and (12), the output signals of two integrators ($v_1(z)$ and $v_2(z)$) are the functions of $x(z)$, the input signal to the converter. Then the signal swing at the output of amplifiers becoming large which makes their implementation in the low-voltage more difficult. The harmonics generated by the amplifier non-linarites also depends on the signal swing of integrator, which severely reduces the SNDR (signal-to-noise and distortion) of the converter with feedback topology.

### Feedforward Topology

The output of the feedforward converter as shown in fig.(2b) can be expressed as [6]:

$$y(z) = x(z) + v_1(z) + v_2(z) + q(z) \qquad (13)$$

The output signals of the first and second integrators ($v_1(z)$ and $v_2(z)$) are as follows:

$$v_1(z) = -z^{-1}(1-z^{-1})q(z) \quad (14)$$

$$v_2(z) = -z^{-2}q(z) \quad (15)$$

Equations (14) and (15) shows that the output signals of two integrators ($v_1(z)$ and $v_2(z)$) are without the input signal $x(z)$, which means that the feedforward converter processes quantization error only. Substituting equations (14) and (15) by equation (13), the loop output is determined as:

$$y(z) = x(z) + q(z)(1-z^{-1})^2 \quad (16)$$

$$STF = 1 \quad (17)$$

$$NTF(z) = (1-Z^{-1})^2 \quad (18)$$

Compared with feedback topology, the NTF given by equation (18) is the same as equation. (5), while the STF is unity under ideal circumstances and not delayed.

Therefore, the signal swings passing through the integrator are smaller and the distortion generated by the non-linearities effect of the amplifiers is input signal independent. It can be significantly reduced. Furthermore, in this topology, the signal amplitude of the amplifiers is reduced and that eases implementation of amplifier design. However, it is more suitable for low-power applications.

## PROPOSED HYBRID ARCHITECTURE OF FEED-FORWARD/ FEEDBACK ADC

### Proposed Converter Architecture

In this paper, a combination of feedforward topology and feedback topology is proposed. The general structure of the proposed (I) feedforword/feedback second order single loop converter is shown in fig.(2c). The input and output of the proposed feedforward/feedback oversampling ADC can be expressed as:

$$u_1(z) = x(z) - y(z) \quad (19)$$

$$v_1(z) = u_1(z).b + v_1(z).z^{-1} \quad (20)$$

$$v_1(z)(1-z^{-1}) = u_1(z).b \quad (21)$$

$$v_1(z)(1-z^{-1}) = x(z).b - y(z).b \quad (22)$$

$$v_1(z) = \frac{x(z).b - y(z).b}{(1-z^{-1})} \quad (23)$$

$$u_2(z) = v_1(z) - y(z).b \quad (24)$$

$$v_2(z) = u_2(z) + v_2(z).z^{-1} \quad (25)$$

$$v_2(z)(1-z^{-1}) = u_2(z) \quad (26)$$

$$v_2(z)(1-z^{-1}) = v_1(z) - y(z).b \quad (27)$$

$$v_2(z) = \frac{v_1(z) - y(z).b}{(1-z^{-1})} \quad (28)$$

$$\therefore v_2(z) = b.\frac{x(z) - y(z).(2-z^{-1})}{(1-z^{-1})^2} \quad (29)$$

Combining the outputs of the modulators as shown in fig.(2c), the output of the entire stage is given by:

$$y(z) = v_1(z).b + v_2(1+b) + x(z) + q(z) \quad (30)$$

Substituting equations (23) and (29) in equation (30), and assume b=1, the final output is given by:

$$y(z) = x(z).\frac{(4-3z^{-1}+z^{-2})}{(6-5z^{-1}+z^{-2})} + e(z).\frac{(1-z^{-1})^2}{(6-5z^{-1}+z^{-2})} \quad (31)$$

The SNR of the proposed architecture is [5]:

$$SNR = 10\log_{10}(\frac{S_q^{\ 2}}{S_e^{\ 2}}) + 10\log_{10}(OSR)dB \quad (32)$$

Where: $s_e^2 = \Delta^2/12$, $\Delta$ =step size of quantizer.

Fig.(3) shows the proposed architecture of feedforward/feedback oversampling ADC with proposed error cancelation circuit at the output. It is a 1-bit quantizer second-order structure with single-loop topology. The proposed novel (I) architecture has following features:

1. The feedforward and feedback signals are summed at the output of the first integrator, and then fed to the second integrator stage.
2. The summation point of feedforward paths before the quantizer in fig.(3a), is necessary to realize all the feedforward signals summed together, which creates feedforward/feedback oversampling ADC.
3. The gain coefficients (b) is chosen for maximizing peak SNDR best performance, and maintain loop stability of the converter. Another consideration in choosing the gain is to guarantee that the baseband quantization noise is independent of the input signal, thereby avoiding the presence of harmonics in the noise floor and decreasing the SNDR, since the harmonics are evident when $b \geq 3$ [7].
4. The drawback of multi-bit quantizer is the need for high linearity in the feedback digital-to-analog converter (DAC). Unfortunately, much of the power savings of multi bit quantization are lost owing to the complexity of the techniques that must be used to linearize the output of this DAC. According to this, a second order single-loop topology with one-bit quantizer has been chosen in this paper, in order to reduce the complexity (no needed for data weighted averaging (DWA) technique in feedback path to reduce the linear error caused by the DAC as design in Ref.[8]) and power dissipation that has more benefits than the higher order and cascade modulators for implementation [9].

**Error Cancellation Circuit (ECC)**

An error cancellation circuit is proposed for single loop high-order in order to eliminate any distortions introduced by the quantization stage. The digital cancellation circuit, as shown in fig.(3b), is required to combine multi input and to eliminate of in-band quantization noise and tone at output of converter. The in-band error quantization noise is shaping to out-of-band by using a second order NTF of ECC. The input and output of the proposed ECC can be expressed as:

$$Out(z) = y(z).z^{-2} + (1-z^{-1})^2.(y(z).z^{-1} + \frac{1}{b}.q(z)) \qquad (33)$$

And the final output of ECC is:

$$Out(z) = y(z).(z^{-1} - z^{-2} + z^{-3}) + \frac{1}{b}.(1-z^{-1})^2.q(z)) \qquad (34)$$

The NTF of proposed ECC is:

$$NTF = (1 - Z^{-1})^2 \qquad (35)$$

**Decimation Filter**

The decimation filter has following features [10]:

1. Remove shaped quantization noise: The modulator is designed to suppress quantization noise in the baseband. Thus, most of the quantization noise is at frequencies above the baseband. The main objective of the digital filter is to remove this out-of-band quantization noise. This leaves a small amount of baseband quantization noise and the band-limited input signal component. Reducing the baseband quantization noise is equivalent to increasing the effective resolution of the digital output.
2. Decimation (sample rate reduction): The output of the modulator is at a very high sampling rate. After the high frequency quantization noise is filtered out, it is possible to reduce the sampling rate. It is desirable to bring the sampling rate down to the Nyquist rate which minimizes the amount of information for subsequent transmission, storage, or digital signal processing (DSP).
3. Anti-aliasing: The input signals are seldom completely band-limited. Since the modulator is sampling at a rate much higher than the output Nyquist rate, the anti-aliasing filter before the modulator can provide the necessary additional aliasing rejection for the input signal as opposed to the internally generated quantization noise.

The simplest and most economical filter to reduce the input sampling rate is a comb-filter because is not require a multiplier. A multiplier is not required because the filter coefficients are all unity.

The transfer function of a comb-filter is [11]:

$$H(z) = \left( \sum_{i-0}^{N-1} z^{-i} \right)^M = \left( \frac{1 - z^{-N}}{1 - Z^{-1}} \right)^M \qquad (36)$$

Where: $N$ is the decimation ratio and $M$ is the order of comb filter.

The algorithm for implementing comb filters is the recursive algorithm. The recursive algorithm with an IIR filter followed by a FIR filter as shown in fig.(3c) [11].

The flow chart of program is shown in fig.(4).

## SIMULATION RESULTS

### Without Decimation Filter

This section presents the simulation of proposed second-order feedforward/feedback ADC without using decimation stage at low OSR, which is suitable for broadband applications [12]. A sinusoidal input with amplitude of 0.7V and a frequency of 1.94 KHz is used. The requirement of the proposed system is summarized in table (1).The measured SNR (by using MATLAB) is 170 db which is equivalent to 28-bit of resolution (by using equation (9)). Fig.(5) shows the quantization noise of the output modulator (y) and the in-band quantization noise error (q). An ECC is proposed for single loop high order modulator to noise shaping the quantization noise of the converter. Fig.(6) shows the in-band noise is perfectly cancelled by using the ECC in output of modulator. Fig.(7) shows the SNR and ENOB versus various input signal power. The final result of simulation of the proposed system is summarized in table (2).

### With Decimation Filter

The decimation filter is accomplished by using the MATLAB function (decimate.m).The basic requirement of the proposed system is summarized in table (2). Fig.(8) shows the quantization noise of the output modulator (y) and the in-band quantization noise error (q). An ECC is proposed for single loop high order to noise shaping the quantization noise of the modulator. Fig.(9) shows the in-band noise is perfectly cancelled by using the ECC in output of modulator. Simulation results show an improvement of 139db (by using MATLAB) in SNR at the output of the converter instead of 86 db was design in Ref.[13] and 75 db was design in Ref.[14]. The resolution or ENOB is 22-bit (by using equation (9)). Fig.(10) shows the SNR and ENOB versus various input signal power. The histogram of output of integrators is shown in fig.(11). The output of quantizer is shown in fig.(12). The final result of simulation of the proposed system is summarized in table (4).

## CONCLUSIONS

In this paper a second order analog-to-digital converter type (single-loop high order) with novel feedforward/feedback architecture has been designed and simulated. With high OSR=256, the net improvement in quantization noise reduction is 64 db if compared with feedforward architecture (single-loop second order) was designed in Ref.[6].The achieved resolution (28-bit) instead of (14-bit) was designed in Ref.[6]. The achieved resolution (28-bit) gives superior performance and suitable to broadband communication applications.

With low OSR=24, the SNR is improved about 55 db if compared with traditional architecture (single-loop third order) was designed in Ref.[13] and 64db if compared with Ref.[14]. The achieved resolution (22-bit)

instead of (14-bit and 12-bit) was designed in Ref.[13] and Ref.[14], respectively.

Finally only one bit quantizer is used in the proposed architecture which greatly decreases the circuit implementation complexity and power consumption.

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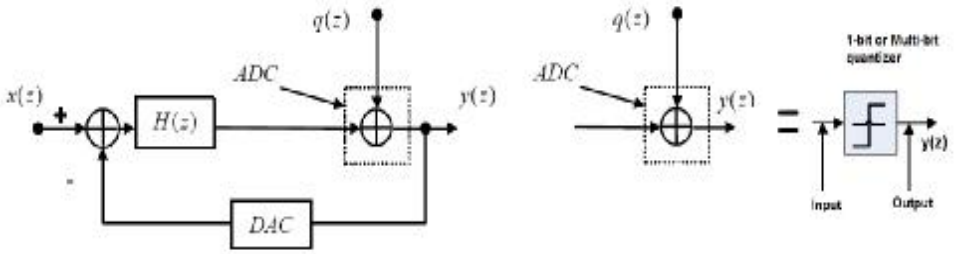
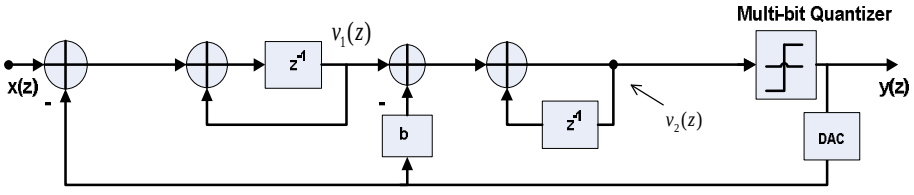



**(a)** **(b)**

**Figure (1): (a) First order oversampling ADC, (b) quantizer [5].**

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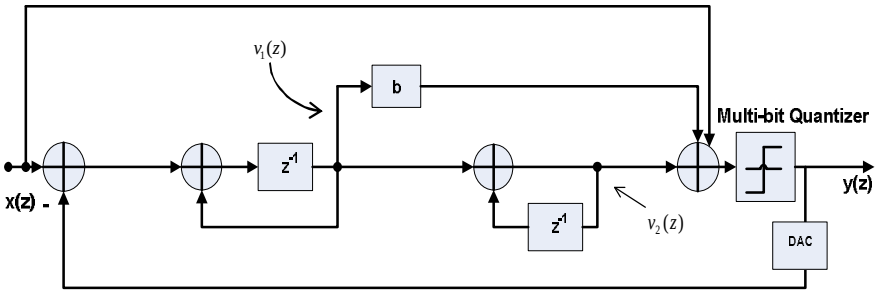


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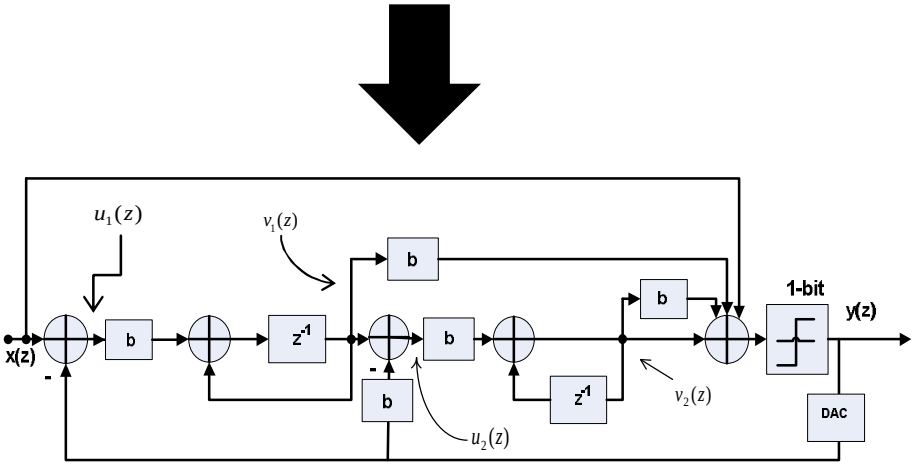
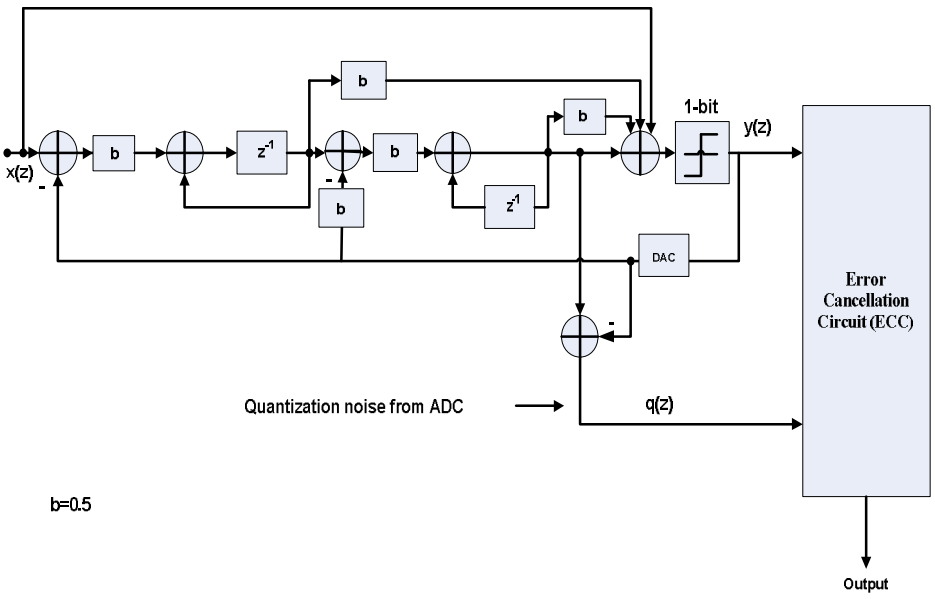



**(c)**

**Figure (2): (a) Conventional feedback second order single loop [6], (b) feedforward second order single loop [6] (c) Proposed hybrid (I) feedforword/feedback second order single loop modulator.**

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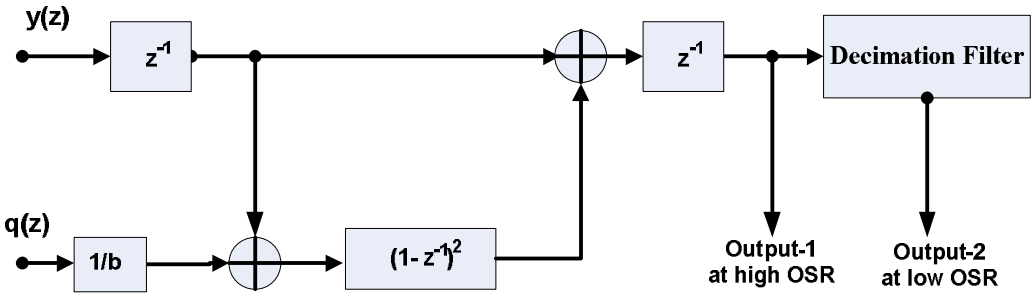


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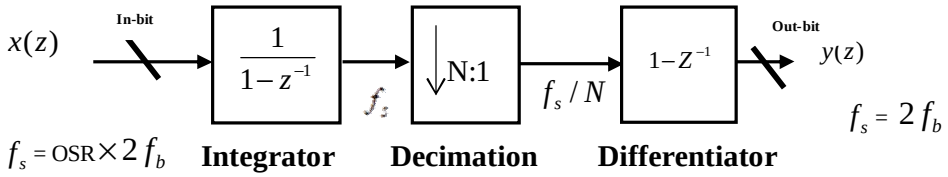



**(c)**

**Figure(3): Proposed architecture (a) Proposed hybrid (I) feedforword/feedback ADC type (second order single-loop) with ECC, (b) Proposed (II) error cancellation circuit (ECC) with decimation filter, (c) Block diagram of one-stage comb-filter [11,12].**

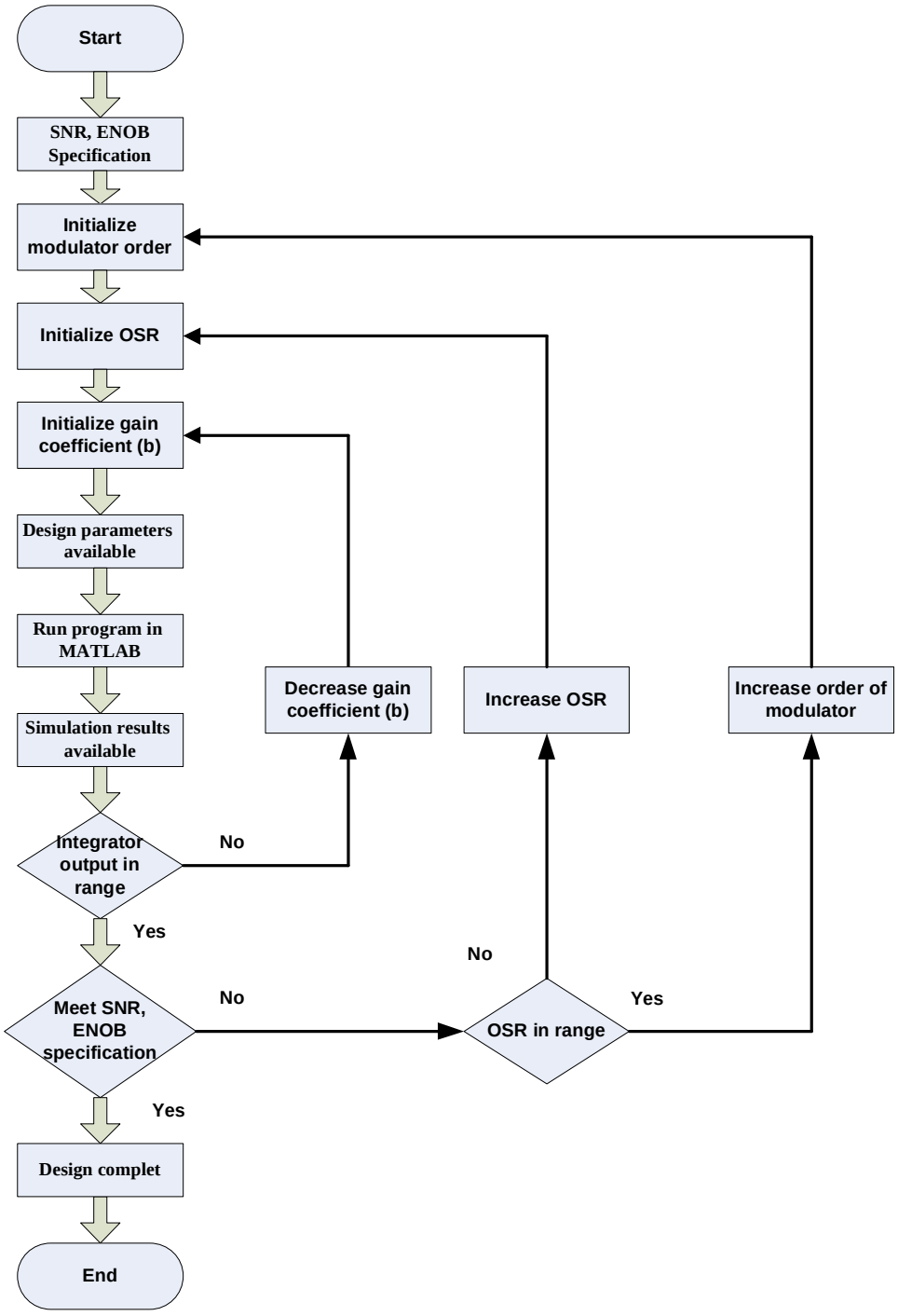



**Figure (4): Flow chart of the simulation program.**

**Table (1): The basic requirements of proposed oversampling ADC.**

| Unit | Parameters | This work | Ref.[6] |
|---|---|---|---|
| **ADC** | Order | Second | Second |
| | Type | Feedforward/Feedback Single-loop | Feedforward Single-loop |
| | OSR | 256 | 256 |
| | Input signal frequency | 1.94KHz | 1.94KHz |
| | Sampling frequency | 1.24MHz | 1.24MHz |
| | Bandwidth | 2KHz | 2KHz |
| | Input signal level | -7dB | Not defined |

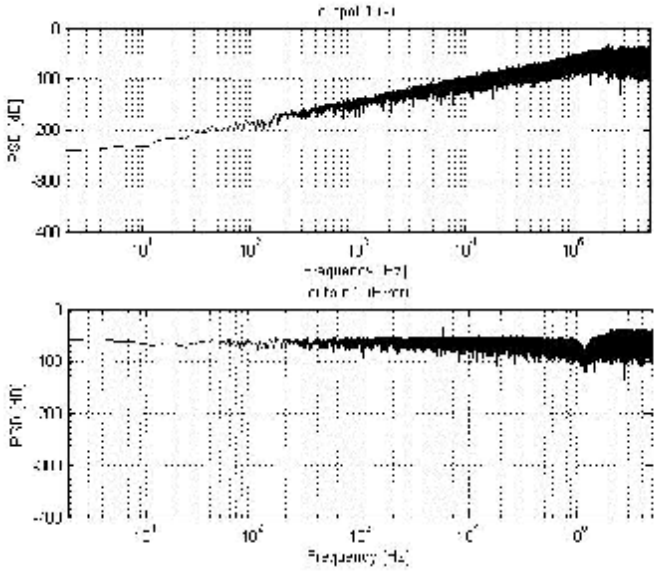


**Figure (5): Simulation of quantization noise spectrum of the modulator (y) And in-band error quantization noise ( $q(z)$ ).**

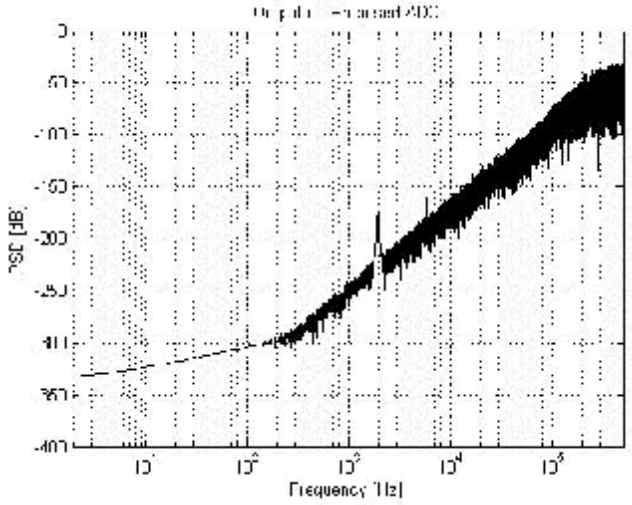
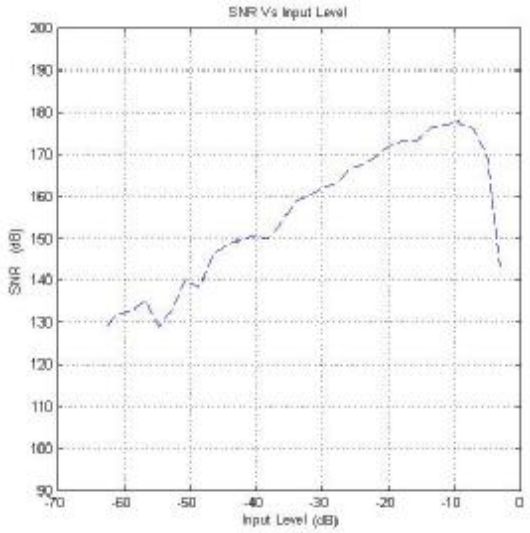
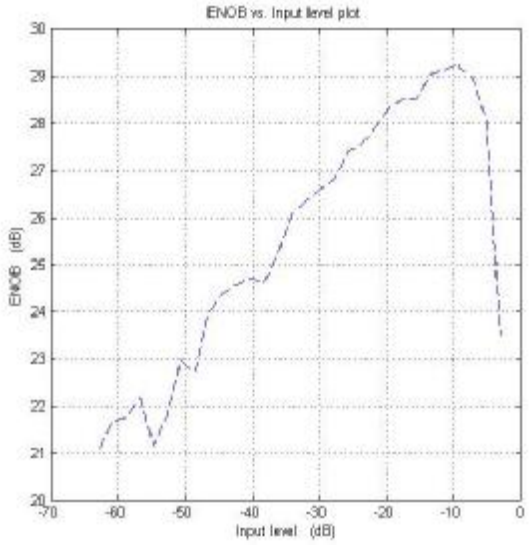



**Figure (6): Simulation of quantization noise spectrum of the proposed novel ADC without decimation stage.**




**(a)**




**(b)**

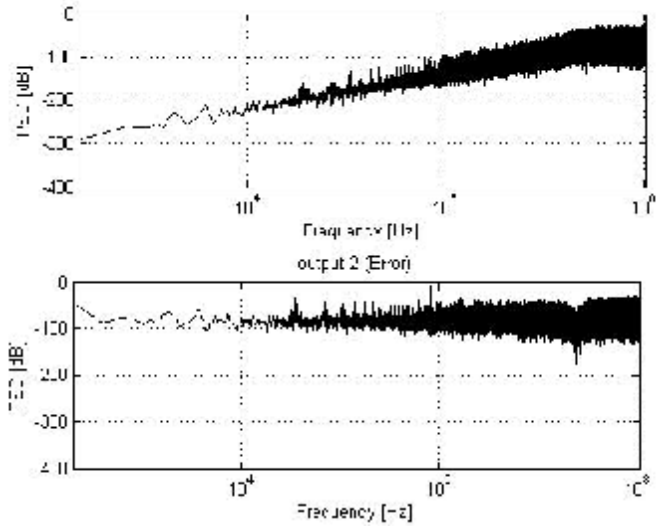
**Figure(7): (a) The SNR versus the input signal power, (b) The ENOB versus the input signal power.**

**Table (2): Summarizes the simulation results.**

| **Parameter** | **This work** | **Ref.[6]** |
|---|---|---|
| **ENOB** | 28-bit | 14-bit |
| **SNR** | 170dB | 106dB |
| **Noise** | -250dB@100KHz | -120dB@100KHz |
| **Order** | Second | Second |
| **Quantizer** | 1-bit | 3-bit |

**Table (3): The basic requirements of proposed oversampling ADC.**

| **Unit** | **Parameters** | **This work without DWA** | **Ref.[13] without DWA** | **Ref.[14] with DWA** |
|---|---|---|---|---|
| **ADC** | order | Second | Third | Third |
| | type | Feedforward/Feedback -Single-loop | Feedback Single-loop | Feedback Single-loop |
| | OSR | 24 | 24 | 24 |
| | Input signal frequency | 825KHz | 825KHz | 825KHz |
| | Sampling frequency | 52.8 MHz | 52.8 MHz | 52.8 MHz |
| | Bandwidth | 1.1MHz | 1.1MHz | 1.1MHz |
| | Input signal level | -7dB | -6dB | -6dB |
| | Decimation filter | Decimation ratio (N)=4 | Not used | Not used |
| | | Order of filter (M) = 30 | | |
| | | Cut-off frequency ($W_n$)=0.25 | | |




**Figure(8): Simulation of quantization noise spectrum of the modulator (y) and in-band error quantization noise ($q(z)$).**

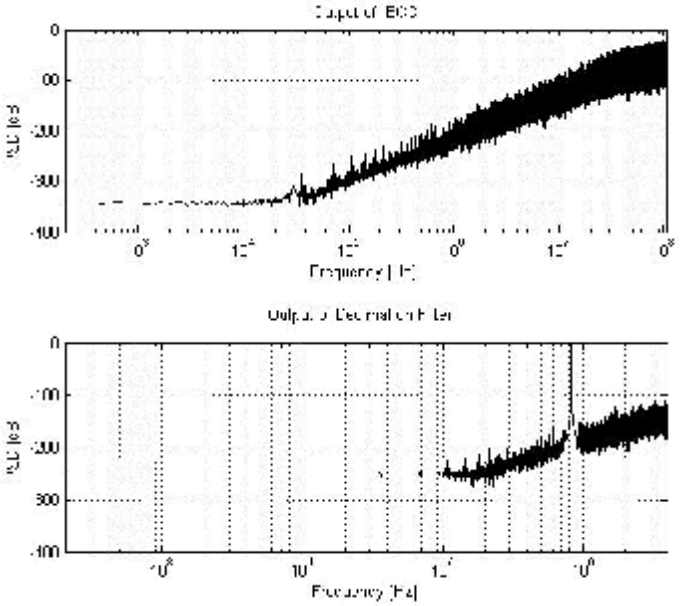
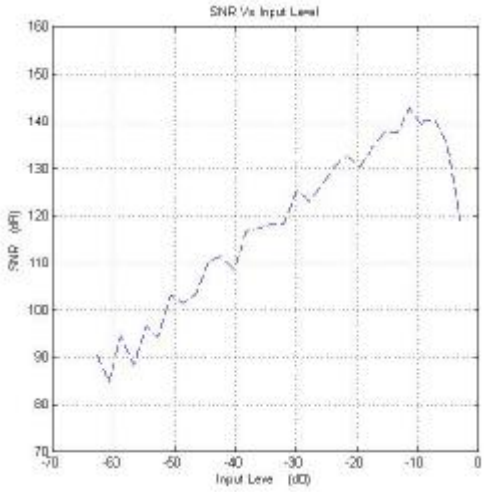
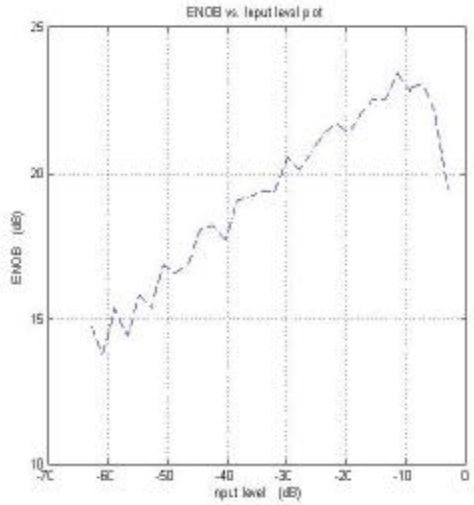



**Figure (9): Simulation of quantization noise spectrum of the ECC and decimation filter.**




**(a)**




**(b)**

**Figure (10): (a) The SNR versus the input signal power, (b) The ENOB versus the input signal power.**

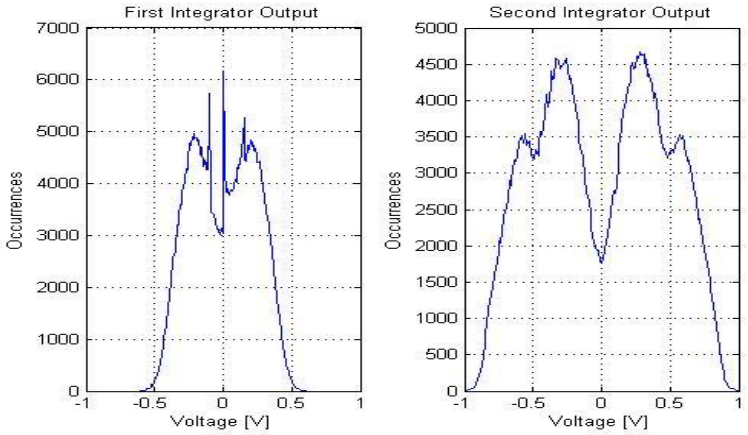



**Figure (11): The output level histograms of the first and second integrators for proposed ADC.**

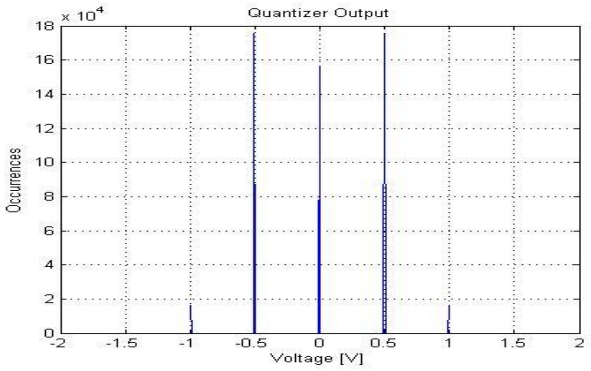



**Figure (12): The output level histogram of quantizer.**

**Table (4): Summarizes the simulation results.**

| Parameter | This work | Ref.[13] | Ref.[14] |
|---|---|---|---|
| **ENOB** | 22-bit | 14-bit | 12-bit |
| **SNR** | 139dB | 84dB | 75 dB |
| **Noise** | -250dB@100KHz | -120dB@100KHz | -100dB@100KHz |
| **Order** | Second | Third | Third |
| **Quantizer** | 1-bit | 3-bit | 3-bit |