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High speed parallel optical adder for quaternary signed-digit number using digit-decomposition-plane representation

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Abstract.

A simple optical scalable parallel and high-speed 2D data array adder for quaternary signed-digit (QSD) number is presented in this paper. The 2D QSD data arrays are coded with the digit-decomposition-plane (DDP) representation. The proposed algorithm performs parallel QSD addition in constant time independent of the size of the QSD data arrays. The methodology design is based on logical formulas which are newly derived to implement optically the suggested QSD adder. The optical implementation of the proposed adder is achieved using classical optical tools to realize the logical formulas. The simulation results of the addition operation insure that the proposed QSD adder works successfully.

Introduction

The parallel computing and high-speed performance systems are the first demand of the processing operation in present days. Most researchers believe that, the optical computing techniques are the solution of this problem, because it provides the parallelism and ultra-high speed computing systems. The important feature of the optical systems is that the optical signals that carry the information can cross each other without occurrence of data corruption. Therefore, the intercommunications between the subunits of

the optical processing systems can link each other with an easy way compared with that of the parallel electronically computing systems [1]. This new technology is called *'' **Optical Computing Systems**''*.

The parallelism of optical processing systems is flexible and not complex in implementation and can process the data in one-dimension and multi-dimension in a small area [2]. Many parallel optical algorithms are suggested and implemented in order to perform the arithmetic operations. Some of these parallel algorithms used the redundant binary numbers, but the other used a multi-leveled number system based on residue arithmetic [3]. A carry-free recoded QSD adder using content addressable memory (CAM) technique is considered in [4]. While a carry-free full parallel optical one-step modified signed-digit (MSD), trinary signed-digit (TSD), and QSD adders using symbolic substutions (SS) technique are studied in [5]. Also optical parallel scalable three-step MSD adder for large-scale two 2D MSD data arrays coded by DDP representation has been studied [6].

In this paper, a parallel optical addition algorithm is proposed for QSD data arrays. The algorithm for addition of two n-digit M×N QSD data arrays generates M×N×(n+1) partial terms, where M is the number of rows and N is the number of columns, while n is the number of QSD digit per one number. The 2D QSD data arrays are coded using digit-decomposition-plane (DDP) coded method. There are two advantages for using DDP representation in optical implementation. The first one is that any DDP plane is the complement of the superimposing plane of the other

planes. The superimposing plane is obtained by accumulating the bright and dark pixels in one plane. The second one is that if all DDP planes are superimposed, the result will be a totally transparent plane. The design describes methodology for obtaining a two-step QSD adder. The QSD addition is described in several combinations newly logical formulas and then implemented using simple classical optical elements, such as beam splitters, mirrors, beam combiners, light sources array, and light detectors array. A simulation example is discussed in order to verify this design.

QSD numbers

In general, a signed decimal number D can be represented in terms of an n-bit radix-r signed-digit number as:

$$D = \sum_{i=0}^{n-1} x_i r^i \qquad (1)$$

For QSD number system, r=4 and the digit x_i is a member of the set $\{\bar{3},\bar{2},\bar{1},0,1,2,3\}$ where $\bar{3}$, $\bar{2}$ and $\bar{1}$ represent -3, -2 and -1 respectively. Since a number may have more than one representation in the signed-digit number, it is also known as a redundant number system. The degree of redundancy usually increases with the increase of the radix. For illustration, consider the following decimal number 19 and its equivalent QSD representation:

$$(01\bar{1}\bar{1})_{QSD} = (010\bar{3})_{QSD} = (02\bar{3}\bar{1})_{QSD} = (1\bar{2}\bar{3}\bar{1})_{QSD}$$

This redundancy enables us to achieve a parallel carry-free addition and a borrow-free subtraction as well as other complex arithmetic operations.

Recoded QSD addition

The two-step adder for QSD numbers is expressed according to the following two equations [5]:

Step 1: $x_i + y_i = 4c_i + s_i \qquad (2)$

Step 2: $s_i + c_{i-1} = z_i \qquad (3)$

Figure 1 presents the block diagram of this adder. Boxes D (first step) add the CP digits (x_i, y_i) of addend number X and augend's number Y, which are both n-digit QSD numbers, to produce the intermediate sum and carry (s_i, c_i) according to the computational rules of Table 1-a. Boxes E (second step) add s_i to c_{i-1}, to obtain the final result z_i depending on computational rules of Table 1-b. There are 49 combinations of CP (x_i, y_i) can be classified into 13 groups which are represented the first step computational rules as shown in Table 1-a.

In the second step, 15 combinations of (s_i, c_{i-1}) are determined and classified into 7 groups $(H_1 - H_7)$ as in the computational rules presented in Table 1-b in order to obtain the final result, which will be (n+1)-digit QSD number.

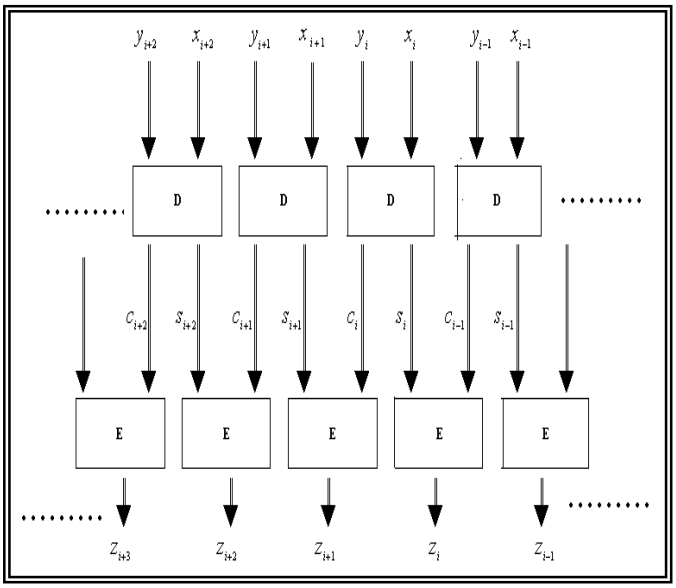


Fig. 1: Block diagram of two-step QSD adder

groups	current pair CP	intermediate results	
G	(x, y)	s	c
G_3	(3,3)	2	1
G_2	(3,2),(2,3)	1	1
G_1	(3,1),(1,3),(2,2)	0	1
G_0	(3,0),(0,3),(2,1),(1,2)	$\bar{1}$	1
G_{-1}	(3,$\bar{1}$),($\bar{1}$,3),(2,0),(0,2),($\bar{1}$,$\bar{1}$)	2	0
G_{-2}	(3,$\bar{2}$),($\bar{2}$,3),(2,$\bar{1}$),($\bar{1}$,2),(1,0),(0,1)	1	0
G_{-3}	(3,$\bar{3}$),($\bar{3}$,3),(2,$\bar{2}$),($\bar{2}$,2),(0,$\bar{1}$),($\bar{1}$,$\bar{1}$),(0,0)	0	0
G_{-4}	($\bar{3}$,2),(2,$\bar{3}$),($\bar{2}$,1),(1,$\bar{2}$),($\bar{1}$,$\bar{1}$),(0,$\bar{1}$)	$\bar{1}$	0
G_{-5}	($\bar{3}$,1),(1,$\bar{3}$),($\bar{2}$,0),(0,$\bar{2}$),($\bar{1}$,$\bar{1}$)	$\bar{2}$	0
G_{-6}	($\bar{3}$,0),(0,$\bar{3}$),($\bar{2}$,$\bar{1}$),($\bar{1}$,$\bar{2}$)	1	$\bar{1}$
G_{-7}	($\bar{3}$,$\bar{1}$),($\bar{1}$,$\bar{3}$),($\bar{2}$,$\bar{2}$)	0	$\bar{1}$
G_{-8}	($\bar{3}$,$\bar{2}$),($\bar{2}$,$\bar{3}$)	$\bar{1}$	$\bar{1}$
G_{-9}	($\bar{3}$,$\bar{3}$)	$\bar{2}$	$\bar{1}$

a

groups	intermediate results	final results
H_i	(s_i, c_{i-1})	z_i
H_3	(2,1)	3
H_2	(2,0),(1,1)	2
H_1	(2,$\bar{1}$),(1,0),(0,1)	1
H_0	(1,$\bar{1}$),($\bar{1}$,1),(0,0)	0
H_{-1}	($\bar{2}$,1),($\bar{1}$,0),(0,$\bar{1}$)	$\bar{1}$
H_{-2}	($\bar{2}$,0),($\bar{1}$,$\bar{1}$)	$\bar{2}$
H_{-3}	($\bar{2}$,$\bar{1}$)	$\bar{3}$

b

Table. 1: Truth tables for QSD adder

QSD adder with DDP representation

DDP representation has been proposed by *Hongxin Huang* and *et.al* [6]. It is an extension for bit-plane representation method. DDP representation can be applied to code large 2D data arrays of QSD numbers. The two steps described in equations 2 and 3 are used to derive the logical formulas in order to implement QSD adder. The logical formulas of the first and second steps of the QSD array adder are derived based on Table 1. The M×N×n QSD A and B arrays are decomposed each into 7 DDP planes (A3, A2, A1, A0, $A\bar{1}$, $A\bar{2}$, $A\bar{3}$) and (B1, B2, B1, B0, $B\bar{1}$, $B\bar{2}$, $B\bar{3}$).

First-step:

According to Table 1-a, the intermediate sum s_i is equal to 2, if the following rule is matched:

$$IF\ (x_i, y_i) = (3,3)\bar{OR}(2,\bar{0})OR(0,2)\ OR(3,\bar{1})OR(\bar{1},3)OR(1,1)\ THEN\ s_i = 2 \quad (4)$$

Due to the same reasons explained in the previous sections, rule (4) can be rewritten as:

$$s2_{ji} = a3_{ji} * b3_{ji} + a2_{ji} * b0_{ji} + a0_{ji} * b2_{ji} + a3_{ji} * \bar{b1}_{ji} + \bar{a1}_{ji} * b3_{ji} + a1_{ji} * b1_{ji} \quad (5)$$

Also, rule (5) can be rewritten to illustrate the array operation as follow:

$$S2 = A3 * \bar{B3} + \bar{A2} * B0 + A0 * B2 + A3 * \bar{B1} + \bar{A1} * B3 + A1 \quad (6)$$

After simplification, it can be written as:

$$S2 = \bar{A3} * (B3 + \bar{B1}) + A2 * B0 + A0 * B2 + \bar{A1} * B3 + A1 * B1 \quad (7)$$

It is clear that rule (7) calculates the DDP plane S2, which includes the intermediate sums of the first-step addition of A and B QSD arrays that have values 2 in parallel. The remaining seven DDP planes of the intermediate sum array S (S1, S0, $S\bar{1}$, and $S\bar{2}$) and intermediate carry array C (C1, C0, and $C\bar{1}$) can be obtained by using the following seven rules which are derived from Table 1-a:

$$S1 = (A2 + \bar{A2}) * (B3 + \bar{B1}) + (A3 + \bar{A1}) * (B2 + \bar{B2}) + A0 * (B1 + \bar{B3}) + (A1 + \bar{A3}) * B0 \quad (8)$$

$$S0 = (A3 + \bar{A1}) * (B1 + \bar{B3}) + (A1 + \bar{A3}) * (B3 + \bar{B1}) + (A2 + \bar{A2}) * (B2 + \bar{B2}) + A0 * B0 \quad (9)$$

$$S\bar{1} = (A2 + A\bar{2}) * (B1 + B\bar{3}) + (A1 + A\bar{3}) * (B\bar{2} + B2) + A0 * (B\bar{3} + B\bar{1}) + (A3 + A\bar{1}) * B0 \quad (10)$$

$$S\bar{2} = A\bar{3} * (B1 + B\bar{3}) + A\bar{2} * B0 + A0 * B\bar{2} + A1 * B\bar{3} + A\bar{1} * B\bar{1} \quad (11)$$

$$C1 = (A3 + A2) * (B3 + B2 + B1) + A1 * (B3 + B2) + A3 * B0 + A0 * B3 \quad (12)$$

$$C0 = (A3 + A2 + A1) * (B\bar{1} + B\bar{2} + B\bar{3}) + (A\bar{1} + A\bar{2} + A\bar{3}) * (B3 + B2 + B1) + (A2 + A1 + A\bar{1} + A\bar{2}) * B0 + A0 * (B2 + B1 + B\bar{1} + B\bar{2}) + A1 * B1 + A0 * B0 + A\bar{1} * B\bar{1} \quad (13)$$

$$C\bar{1} = (A\bar{2} + A\bar{3}) * (B\bar{1} + B\bar{2} + B\bar{3}) + A\bar{1} * (B\bar{2} + B\bar{3}) + A\bar{3} * B0 + A0 * B\bar{3} \quad (14)$$

Second-step:

The computational rules of QSD 2-step addition are presented in Table 1-b. Here we have eight DDP planes hold the intermediate sum (S2, S1, S0, $S\bar{1}$, $S\bar{2}$) and intermediate carry (C1, C0, $C\bar{1}$). The final results contain seven DDP planes named Z3, Z2, Z1, Z0, $Z\bar{1}$, $Z\bar{2}$, and $Z\bar{3}$.

The first computational rule of Table 1-b can be expressed as:

$$IF\ (s_i, c_{i-1}) = (2,1)\ THEN\ z_i = 3 \quad (15)$$

According to the derivation steps explained in the previous sections, rule (15) above can be expressed as:

$$Z3 = S2 * C'1 \quad (16)$$

Where symbol $(')$ means shifting one position to the left of each number in C1 plane and padding one zero in LSB positions. Now, the Z3 plane holds the digits of the resulting QSD array Z that have values 3 and are represented as bright spots. The rest DDP planes of the final results can be obtained by the following rules:

$$Z2 = S2 * C'0 + S1 * C'1 \quad (17)$$

$$Z1 = S2 * C'\bar{1} + S1 * C'0 + S0 * C'1 \quad (18)$$

$$Z0 = S1 * C'\bar{1} + S0 * C'0 + S\bar{1} * C'1 \quad (19)$$

$$Z\bar{1} = S\bar{2} * C'1 + S\bar{1} * C'0 + S0 * C'\bar{1} \quad (20)$$

$$Z\bar{2} = S\bar{2} * C'0 + S\bar{1} * C'\bar{1} \quad (21)$$

$$Z\bar{3} = S\bar{2} * C'\bar{1} \quad (22)$$

The result will be seven M×N×(n +1) DDP planes which represent the QSD array of the final results Z.

Proposed optical implementation

The optical QSD array adder can be implemented practically using simple optical tools. The logical AND and OR gates are the main operations in the logical formulas. Logical AND can be constructed optically by cascading two DDP planes, each of one array, with the same dimensions and pixel resolutions as shown in Fig. 2. The light beams are applied on each pixel of the first plane. These beams pass through the transparent pixel (1) and block by opaque pixel (0). While optical logical OR can be constructed by using a beam combiner (BC). BC performs light beams of the two packages that can pass through two DDP planes and fallen onto the two BC input surfaces as shown in Fig. 3. For more information see Reference [6].

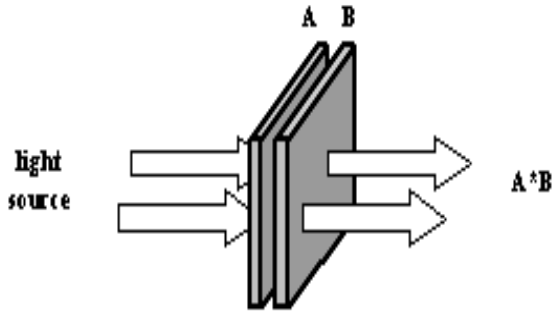


Fig. 2: AND gate optical implementation

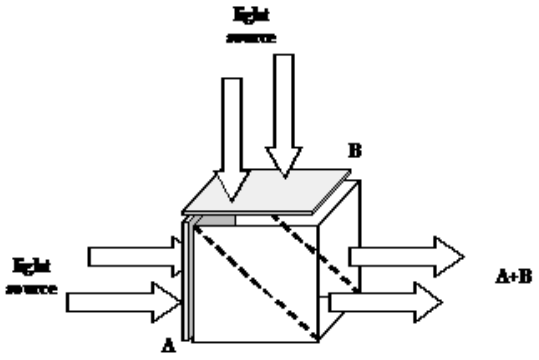


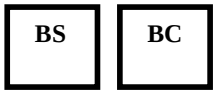
Fig. 3: OR gate optical implementation

The proposed parallel optical two-step QSD adder operation can be explained as follows:

1- The input M×N×n DDP-planes of the first step will be illuminated by Laser sources to enter the optical system for processing.
2- Light detector arrays (LDAs) in the end of optical scheme of the first step will detect the DDP-planes of the intermediate results that are produced by the first step.
3- These optical signals are converted to electrical signals and passed to the optical implementation of the second step.
4- The input DDP-planes of the second step is addressed in parallel by these electrical signals to form the sufficient expanded and shifted copies of the intermediate results. Expanding and shifting mean that one pixel is necessary to be zero padded to the LSB

and MSD pixel position of the detected DDP-planes of the intermediate carry and intermediate sum, respectively.

5- Finally, the LDAs detect the optical signals that represent the DDP-planes in the final result array, which are M×N×(n+1) QSD array. The above points present the complete optical implementation of the suggested parallel optical two-step QSD adder with the consideration of the following explanations:



: denotes a beam combiner and beam splitter.

: denotes a mirror.

: denotes SLM (DDP plane), LDA, or CMP.

: the direction of the light signal emitted by an optical source.

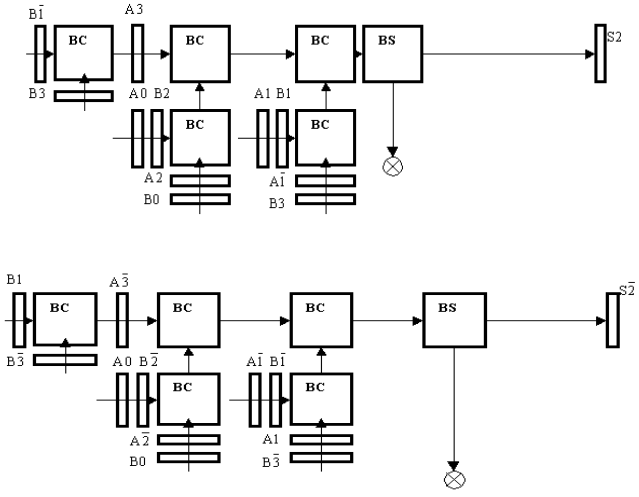
The proposed optical implementation of the two steps 2D QSD array is shown in Fig: 4.

Simulation results

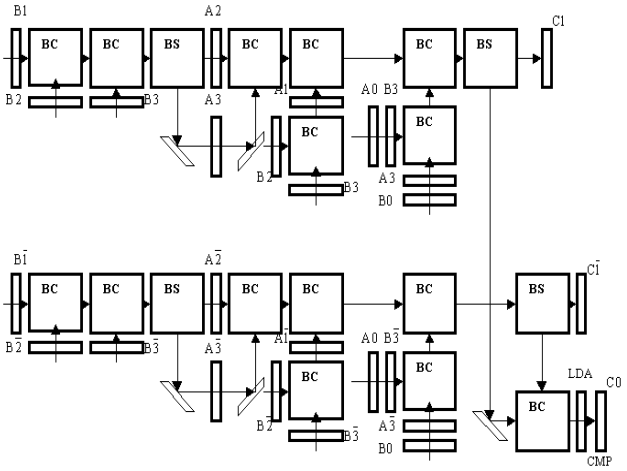
The optical implementation of the proposed two-step QSD array adder with DDP representation is tested here. Two 10×2×4 QSD arrays A and B are added using this adder.

Figure 5 shows the DDP-planes of the input arrays A and B. Also the DDP-planes of the intermediate sum S and carry C arrays, which are calculated by the optical implementation of the first step are presented in Fig. 5. The DDP-planes of the final result array Z are obtained by the optical implementation of the second step of the QSD array adder. Note that the delay time which prevents the speed of the proposed optical system to approach exactly to the speed of the light is caused by two terms:

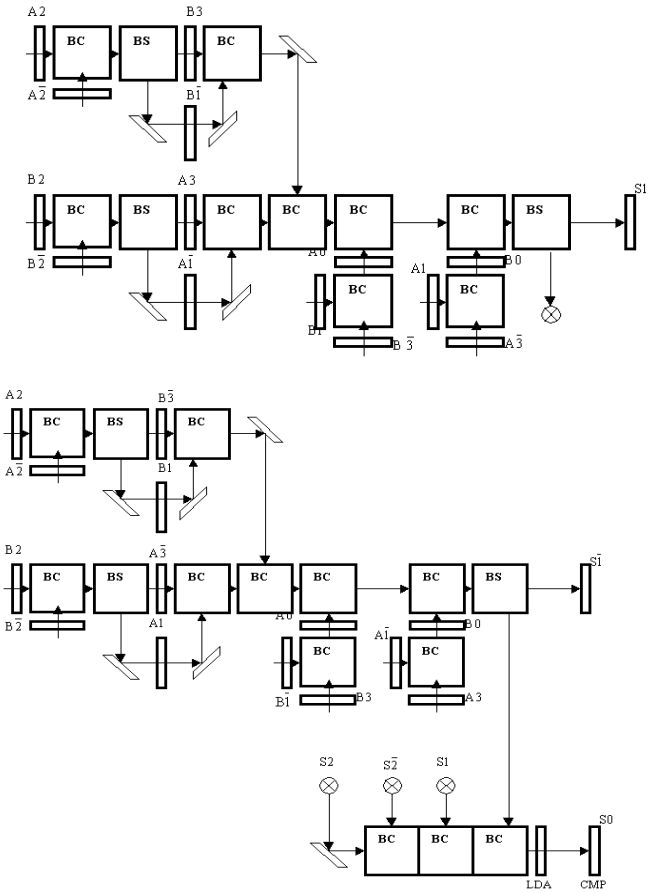
a- The holding time of the input images, and
b- The propagation times of light from the source to detector planes.

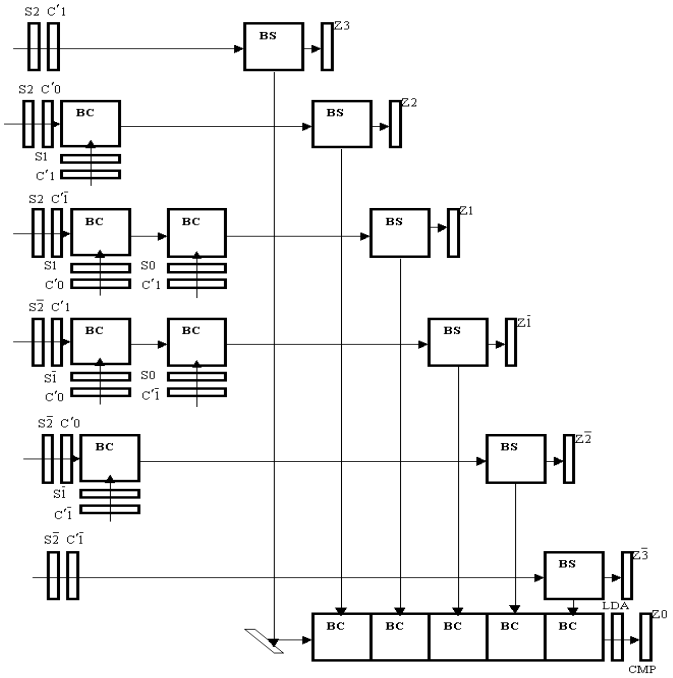


(a)



(b)





(c)

Fig. 4: Optical implementation of the proposed two-step QSD adder
(a) First-Step (intermediate sum generation)
(b) First-Step (intermediate carry generation)
(c) Second-Step (final results generation)

$$A=\begin{bmatrix}255 & 101\\ 132 & 0\\ 50 & 114\\ 31 & 215\\ 193 & -15\\ 172 & 0\\ 247 & -199\\ -76 & 47\\ -89 & -220\\ -255 & 132\end{bmatrix}_{10}=\begin{bmatrix}3333 & 1211\\ 2010 & 0000\\ 0302 & 1302\\ 0133 & 3113\\ 3001 & 00\bar{3}\bar{3}\\ 2230 & 0000\\ 3313 & \bar{3}0\bar{1}\bar{3}\\ \bar{1}0\bar{3}0 & 0233\\ \bar{1}\bar{1}2\bar{1} & \bar{3}\bar{1}\bar{3}0\\ \bar{3}\bar{3}\bar{3}\bar{3} & 2010\end{bmatrix}_{QSD}$$

$$B=\begin{bmatrix}255 & 209\\ 92 & 0\\ -13 & 69\\ -200 & -205\\ -110 & 30\\ 121 & 100\\ -100 & 250\\ 249 & -47\\ -175 & -113\\ -255 & 39\end{bmatrix}_{10}=\begin{bmatrix}3333 & 3101\\ 1130 & 0000\\ 00\bar{3}\bar{1} & 1011\\ \bar{3}0\bar{2}0 & \bar{3}0\bar{3}\bar{1}\\ \bar{1}\bar{2}\bar{3}\bar{2} & 0132\\ 1321 & 1210\\ \bar{1}\bar{2}\bar{1}0 & 3322\\ 3321 & 0\bar{2}\bar{3}\bar{3}\\ \bar{2}\bar{2}\bar{3}\bar{3} & \bar{1}\bar{3}0\bar{1}\\ \bar{3}\bar{3}\bar{3}\bar{3} & 0213\end{bmatrix}_{QSD}$$

$$Z=\begin{bmatrix}13332 & 11\bar{1}12\\ 1\bar{1}200 & 00000\\ 01\bar{2}11 & 03\bar{1}2\bar{1}\\ \bar{1}112\bar{1} & 001\bar{2}2\\ 023\bar{1}\bar{1} & 0010\bar{1}\\ 10211 & 01210\\ 0211\bar{1} & 01\bar{1}\bar{1}\bar{1}\\ 03\bar{1}\bar{1}1 & 00000\\ \bar{1}00\bar{2}0 & \bar{1}\bar{1}\bar{1}\bar{1}\\ \bar{1}\bar{3}\bar{3}\bar{3}2 & 0223\bar{1}\end{bmatrix}_{QSD}=\begin{bmatrix}510 & 310\\ 224 & 0\\ 37 & 183\\ -169 & 10\\ 83 & 15\\ 293 & 100\\ 147 & 51\\ 173 & 0\\ -264 & -333\\ -510 & 171\end{bmatrix}_{10}$$

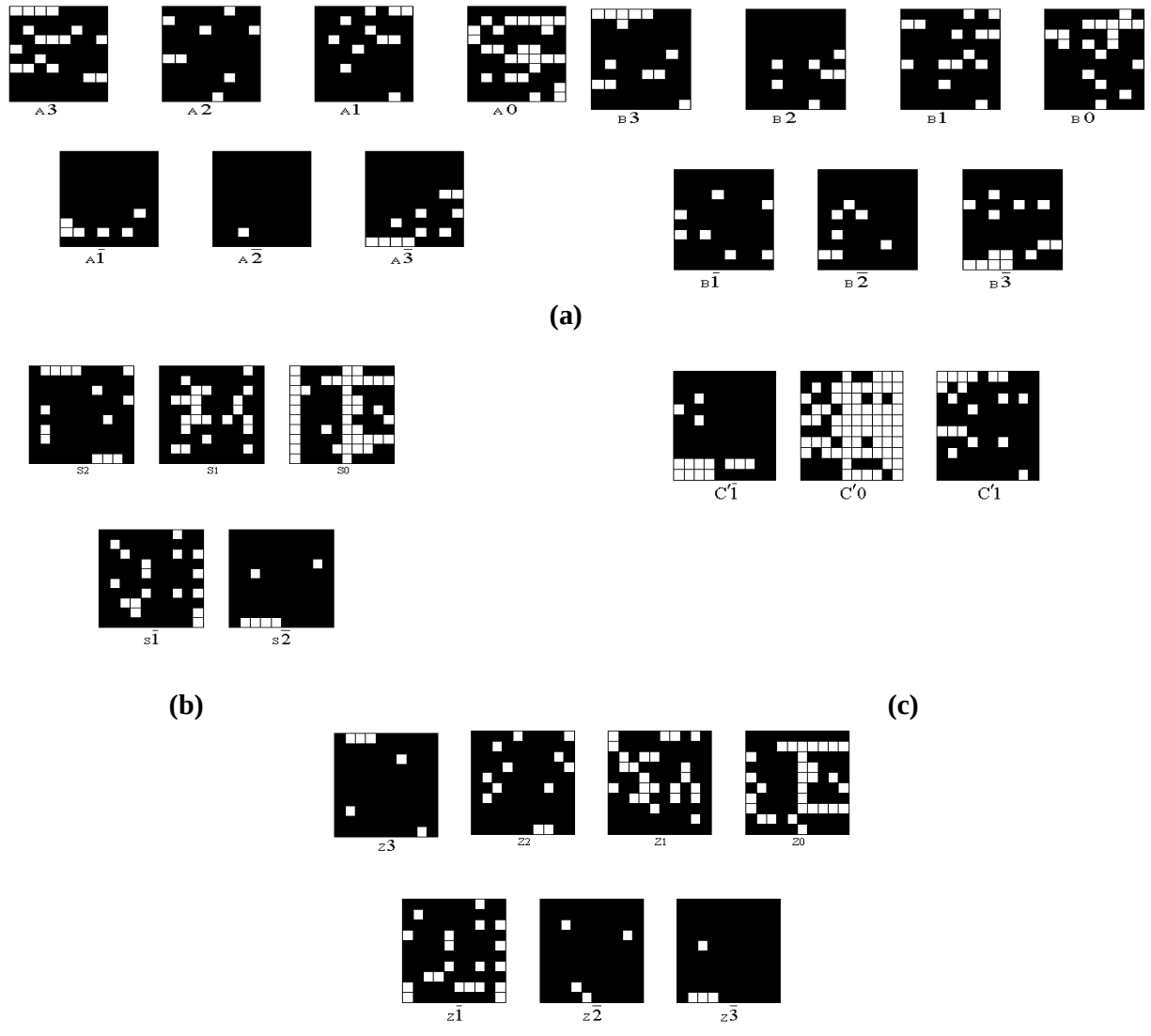


Fig. 5: Simulation results of the proposed two-step QSD adder

(a) A and B SLM inputs

(b) First-Step (intermediate sum generation)

(c) First-Step (intermediate carry generation)

(d) Second-Step (final results generation)

A simulation program is built by using C++ language to test the proposed QSD adder. The propagation time can be ignored because of the whole system hardware is small if the optical tools dimensions are taken into account. While the SLM response time represents the major delay time. The throughputs of the optical adder can be calculated by the following equation:

$$Throughput = \frac{PR}{2R_T} \qquad (23)$$

Where PR and R_T are the pixel resolution and the response time of the SLM type, respectively, that are used in the implementation.

Conclusion

In this paper, an efficient technique for recorded QSD addition is presented. The proposed technique performs parallel QSD addition in constant time. Both methods of algorithms and architectures are independent of the sizes of the operand arrays. An optical implementation scheme was discussed based on classic optical elements such as beam-splitters, mirrors, and parallel plates.

The algorithm and its optical architecture have useful intrinsic characteristics such as no sign, no decimal point, no carry, and scalable computation on large-scale data arrays. A Preliminary experiment based on a hybrid scheme was presented.

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الجامع الضوئي المتوازي ذو السرعة العالية

باستخدام النظام الرباعي المؤشر واعتماد تمثيل مستويات فصل الأرقام

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الخلاصة

الجامع الضوئي المتوازي العالي السرعة لسلسلة ثنائية البيانات من الأرقام المؤشرة الرباعية تم عرضه. شفرت البيانات الثنائية السلسلة من الأرقام المؤشرة الرباعية بتقنية مستويات فصل الأرقام. الخوارزمية المقترحة تنفذ عملية الجمع للأرقام في زمن ثابت ودون الاعتماد على حجم البيانات في الأرقام المؤشرة الرباعية. التصميم اعتمد على معادلات منطقية اشتقت حديثا لغرض بناء الجامع الضوئي المقترح. البناء الضوئي للجامع تم تنفيذه باستخدام الأدوات التقليدية الضوئية بما يحقق المعادلات المنطقية. نتائج المحاكاة لعمليات الجمع تؤكد بان الجامع الأرقام المؤشرة الرباعية يعمل بنجاح.