

SOFT SWITCHING PWM AC/DC CONVERTER

A. S. Alsheraidah R. S. Fyath M. M. Ibrahim

Department of Electrical Engineering
College of Engineering
University of Basrah
Basrah - IRAQ

ABSTRACT

This paper presents a PWM AC/DC buck converter circuit incorporating a frontend rectifier followed by a DC/DC converter. Two transistors are used as a main and auxiliary switches. The proposed circuit provides zero-current (ZC) turn ON and zero-current/zero-voltage (ZCZV) turn OFF to the two transistors, besides zero-voltage turn ON to two diodes. Numerical methods are used to analyse and determine the performance of the converter system. A feedforward technique is employed to improve the performance of the converter over a range of output power.

Key words: AC/DC converter, ZCS and ZVS switching converter.

محول القدرة AC/DC المضمن بعرض النبضة ذو التبديل اللين

د. احمد سليم التريده د. رعد سامي فياض د. مصطفى محمد ابراهيم
قسم الهندسة الكهربائية - كلية الهندسة - جامعة البصرة - البصرة - العراق

المعنى

يقدم البحث دراسة تحليل القدرة AC/DC المخفض للجهد و المضمن بعرض النبضة (PWM) والمكون من مقوم دهرودات متبوع بدائرة مقوم DC//DC. استخدم ترانزستورين كمتحليين، احدهما رئيسي والاخر ثانوي. الدارة المقترحة توفر للترانزستورين حالة الفتح عند تيار جهته صفر (ZCS) و حالة طلق عند تيار و فولتية صفر (ZCZVS) إضافة الى حالة الفتح عند الصفر فولت ادهرودات المقوم. استخدمت طريقة عددية للتطبيق و حساب اداء المسير لمدى من القدرة الاخراج.

1. INTRODUCTION

AC/DC converter circuits are widely used in several industrial applications. The use of rectifier circuit with filter causes a nonsinusoidal current waveform drawn from the AC supply, which contains large total harmonic distortion (THD) and has low power factor. With this distorted current that represents electric power grid pollution, electromagnetic interference, losses in transmission and distribution lines, and voltage distortion are associated [1].

Different topologies of high power factor PWM AC/DC converter circuits but with high voltage and current stresses have been proposed in several papers [1-7]. A family of soft switching, high power factor converters have been proposed in the literatures where zero-voltage-switching (ZVS) or zero-current-switching (ZCS) have been applied during turn OFF or turn ON transition [8-10].

In this paper, a ZCS-PWM soft commutation cell, which has been proposed in [10], is used with a PWM AC/DC converter circuit as shown in Fig.(1). The circuit provides ZCS and ZCZVS during turn ON and turn OFF transitions of the two switching transistors respectively, as well as a ZV turn ON to the diodes. The operation of the converter system is analysed and its performance is determined using fourth-

order Runge-Kutta method incorporating Fourier series and numerical integral techniques. The results indicate clearly that the performance of the converter can be improved by using a feedforward technique. A high power factor and low total harmonic distortion are achieved over a range of output power.

2. CONVERTER OPERATION

The studied PWM AC/DC buck converter circuit is shown in Fig.(1). The soft commutation cell contains two switching transistors (S1-main and S2-auxiliary) with two anti-parallel diodes Ds1 and Ds2 respectively, two resonant inductors Lr1 and Lr2, one resonant capacitor Cr, and two diodes D1 and D2.

The performance of the converter can be analysed by dividing its operation during each switching period time ($T_s = 1/F_s$) into nine topological stages, as shown in Fig.(2). Fig.(3) shows the time interval diagram of one switching period.

Stage-1

This stage continues during the time interval ($T_0 < t \leq T_1$). At the beginning D1 and D2 are conducting and S1 starts to conduct. The resonant inductor current $I(Lr1)$ starts from zero satisfying ZCS for the switching transistor S1. This stage continues until the current $I(Lr1)$ reaches the smoothing

inductor current i_L . The following equations are used to describe the operation of this stage.

$$L \frac{di_L(t)}{dt} = -V_o(t) \quad \text{-----(1)}$$

$$i_L(t) = C \frac{dV_o(t)}{dt} + V_o(t)/R \quad \text{-----(2)}$$

$$V_i(t) = Lr1 \frac{di(Lr1)(t)}{dt} \quad \text{-----(3)}$$

where V_i and V_o are input and output voltages, respectively.

Stage-2

When the resonant inductor current $i(Lr1)$ reaches the inductor current i_L , the two diodes D1 and D2 are turned OFF, making stage-1 ended and starting stage-2. This stage operates over the time interval $T1 < t \leq T2$ and its performance can be described by equations 2 and 4.

$$V_i(t) = (L + Lr1) \frac{di_L(t)}{dt} + V_o(t) \quad \text{-----(4)}$$

The time interval of this stage depends on the duty cycle of the converter (D), i.e. when $T2 - T_0 = DT_s$, where T_s is the switching period time ($T_s = 1/F_s$) and F_s is the switching frequency of the converter. During this stage, the AC input supply is connected to the load (R) through the smoothing inductor (L) and Lr1.

Stage-3

To turn OFF the main switching

transistor S1, the auxiliary switching transistor S2 is turned ON and the resonant inductor current $i(Lr2)$ starts from zero, satisfying ZCS to the auxiliary switch S2.

At that time ($t = T2$), the resonant capacitor C_r discharges through the resonant inductor Lr2. This stage is valid until the voltage of the resonant capacitor reaches zero ($V_{cr} = 0$) at $t = T3$. The time duration of this stage is $T2 < t \leq T3$ and the operation of the converter can be described by equations 2 and 4-6.

$$Lr2 \frac{di(Lr2)(t)}{dt} = V_{cr}(t) \quad \text{-----(5)}$$

$$C_r \frac{dV_{cr}(t)}{dt} = -i(Lr2)(t) \quad \text{-----(6)}$$

Stage-4

When the resonant capacitor voltage (V_{cr}) reaches zero, diode D1 starts conducting at zero voltage satisfying ZVS condition. The resonance occurs among the two resonant inductors (Lr1 and Lr2). The operation of this stage continues until $i(Lr1)$ reaches zero, i.e. the main switching transistor S1 is turned OFF with ZCS and at the same time with ZVS, because Ds1 starts conducting (turns ON). The operation time interval of this stage is $T3 < t \leq T4$ and equations 2, 5 and 7-9 describe its operation.

$$L \frac{di_L(t)}{dt} = V_i(t) - V_o(t) - V_{cr}(t) \quad \text{-----(7)}$$

$$C_r \frac{dV_{cr}(t)}{dt} = i_L(t) - i(Lr1)(t) - i(Lr2)(t) \quad \text{-----(8)}$$

$$Lr1 \frac{dI(Lr1)(t)}{dt} = Vcr(t) \quad \text{-----}(9)$$

Stage-5

At time $t=T4$, the switching transistor S1 is turned OFF and the anti-parallel diode Ds1 starts conducting. The operation of this stage continues until the resonant inductor current $I(Lr2)$ reaches zero. At this time, the auxiliary switching transistor S2 is turned OFF at zero current condition, while the anti-parallel diode Ds2 starts conducting (turns ON) providing zero voltage switching condition to the switch S2. The time interval of this stage is $T4 < t \leq T5$ and its operation can be described by equations 2,5 and 7-9.

Stage-6

This stage starts when the anti-parallel diode Ds2 is turned ON. The operation of this stage continues until the resonant inductor current $I(Lr2)$ reaches zero. At this time the diode Ds2 is turned OFF. The time interval of this stage is $T5 < t \leq T6$ and the equations of stage-5 can be used to describe the operation of this stage.

Stage-7

This stage starts with the two switches S1 and S2, and the anti-parallel diode Ds2 are turned OFF during the previous stages. The resonant current flows through Ds1 only. This stage continues

until the resonant current $I(Lr1)$ reaches zero and the diode Ds1 is switched OFF. The interval operation of this stage is $T6 < t \leq T7$ and equations 2,7,9 and 10 are describing the operation of this stage.

$$Cr \frac{dVcr(t)}{dt} = I_L(t) - I(Lr1)(t) \quad \text{-----}(10)$$

Stage-8

In this stage, the resonant capacitor, Cr , is charging through the input supply until the diode D2 starts conducting. The time interval of this stage is $T7 < t \leq T8$ and the operation of this stage can be described by equations 2,7 and 11.

$$Cr \frac{dVcr(t)}{dt} = I_L(t) \quad \text{-----}(11)$$

Stage-9

This stage starts when the diode D2 is turned ON at ZVS and the inductor L is freewheeling through the load and the two diodes D1 and D2. The operation of this stage is performed during the interval time $T8 < t \leq T9$, i.e. until the end of the switching time period is reached ($T9 = Ts$). Equations 1 and 2 describe the operation of this stage.

3.ZERO CURRENT SWITCHING CONDITIONS

To obtain zero-current switching, the following constraints and conditions must be assisted according to the stages of operation as described in section-2 [9-12].

$$\beta = Lr2/Lr1 < 1 \quad \text{-----(12)}$$

$$\alpha = (Io/Vi) (Lr2/Cr)^{1/2} \quad \text{-----(13)}$$

$$\Delta ts2 = \{1 + 2/(1+\beta)^{1/2}\} / (4 Fo) \quad \text{-----(14)}$$

$$Fo = 1/(2\pi (Lr2 Cr)^{1/2}) \quad \text{-----(15)}$$

Here, I_o is the load current and $\Delta ts2$ is the time interval used to control S2. It can be noted that $\Delta ts2$ in equation 14 depends on the resonant parameters only ($Lr1$, $Lr2$, Cr).

4. CONTROL SYSTEM

To regulate the output voltage and to improve the input power factor and the total harmonic distortion (THD) of the converter input current, a feedforward technique is used [13,14] as shown in Fig.(4-a). The output voltage (V_o) of the converter is sensed with a gain of K_o , and then controlled with a reference input voltage (V_r) through a proportional plus integral (PI) controller circuit. The input current of the converter is sensed, gained by a factor K_i , and subtracted from the output of the PI controller. The output of the subtractor (V_c) control a PWM circuit to generate two gate signals (V_{gs1} and V_{gs2}) which are used to switch ON the main and the auxiliary switches (S1 and S2). The control circuit used to generate these two signals is shown in Fig.(4-b).

The control signal $V_c(t)$ can be determined by equation (16)

$$V_c(t) = \{K_o V_o(t) - V_r\} K_p + K_{in} \int \{K_o V_o(t) - V_r\} dt - K_i I_{in}(t) \quad \text{-----(16)}$$

where :

K_p = proportional gain of the PI controller.

K_{in} = integral gain of the PI controller.

I_{in} = converter input current.

5. DESIGN PROCEDURE

The PWM AC/DC buck converter designed parameters are selected and determined as follows:

(1) The input AC voltage is 220V (rms) and the switching frequency $F_s=25$ kHz. The output voltage is kept at 120V when feedforward technique is used.

(2) The resonant parameters ($Lr1$, $Lr2$ and Cr) and the time interval used to control the auxiliary switch ($\Delta ts2$) are determined using equations 12-15 by selecting suitable values for and frequency ratio (F_s/F_o).

Taking the following parameters:

$V_i=220$ V (rms), $V_o=120$ V, $P_o=1600$ W, $F_s=25$ kHz, $\beta=0.8$, $\alpha=0.4$, and $F_s/F_o=0.2$, the values of the resonant inductors and capacitor can be obtained as follows:
 $Lr1 = 10\mu$ H, $Lr2 = 8\mu$ H, and $Cr = 183$ nF.

The time interval used to control the auxiliary switch is $\Delta ts2 = 5\mu$ s.

(3) The output filter parameters L and C are specified by assuming that the output current and voltage are smoothing during the switching period [14]. For that, let $L=1\text{mH}$ and $C=1000\mu\text{F}$.

6. RESULTS

The performance of the converter system at open loop condition (i.e. without feedforward technique) is obtained using equations (1-11). These equations are solved numerically using forth-order Runge-Kutta method which incorporates Fourier series and numerical integral techniques [15]. Fig.(5) shows the variation of the output voltage against load resistance for different values of β and frequency ratio (F_s/F_o) and at a duty cycle $D=0.1$. It can be seen that there are small variations introduced in the output voltage when β and F_s/F_o are varied. The power factor and the THD of the input current are plotted against load resistance in Figs. 6 and 7, respectively, and for the same values of β and F_s/F_o used in Fig.(5). While Fig.(8) depicts the efficiency of the converter as a function of load resistance. Investigating Figs.5-8 reveals that $\beta=0.8$ and $F_s/F_o=0.2$ are suitable parameters to realize the converter because the performance of the system is the best at these values when THD and power factor are considered. At $\beta=0.8$, $F_s/F_o=0.2$, $R=12\Omega$, the converter is characterized by:

Output voltage = 120V
 Input power factor = 0.97
 Input THD = 0.25
 Efficiency = 45%

We carry the calculations further to investigate the influence of the duty cycle on converter performance. The results are displayed in Figs.(9) - (12) as a function of load resistance and assuming $\beta=0.8$ and $F_s/F_o=0.2$. It is clear from these figures that the performance of the converter depends on the load resistance and the duty cycle. Increasing the load resistance or duty cycle reduces the power factor while increases both THD and efficiency. Table-1 lists the main characteristics of the converter obtained at $\beta=0.8$ and $F_s/F_o=0.2$ and taking R and D as independent parameters.

Table-1.

D	0.1			0.2			0.3		
	10	20	40	10	20	40	10	20	40
PF	0.97	0.94	0.88	0.97	0.93	0.87	0.96	0.92	0.85
THD	0.24	0.37	0.53	0.26	0.40	0.57	0.30	0.42	0.60
Efficiency(%)	42	55	66	45	58	68	50	61	70

To improve the performance of the converter, a feedforward technique is used, as shown in Fig.(4). The operation of the converter system is described now by

equations (1-11) in addition to equation (16). These equations are solved numerically using the same technique adopted in the open loop condition. The performance of the converter system is depicted in Figs(13)-(15) when $\beta=0.8$ and $F_s/F_o=0.2$ and for different values of input current gain (K_i). It can be seen from these figures that the converter can operate at output voltage $V_o=120V$ over a range of output power (from 1100W to 2300W), while the converter rated output power as selected in the design procedure is 1600W. The performance of the converter have not the same effect during all this range of output power as shown in these figures. The variation of K_i above 0.4 improves the power factor and the THD but reduces the efficiency, when the converter operated at output power less than the rated value. The input current and voltage waveform of the converter are shown in Fig.(16) which shows that the power factor is high and the THD is comparable low.

7.CONCLUSIONS

A PWM AC/DC converter circuit with high power factor and soft switching has been studied. The circuit offers zero current turn ON and zero current/zero voltage turn OFF for the two switching transistors. The two diodes D1 and D2 are switched ON at zero voltage condition. The performance of the converter has been

examined at open loop and with feedforward technique using forth-order Runge-Kutta method, which incorporated Fourier series and numerical integration methods. The converter can operate satisfactory over a range of output power 0.68 to 1.44 of the selected designed level.

REFERENCES

- [1] A. F. De Souza and I. Barbi, "Comparative analysis of three high power factor single phase 200W rectifiers", 5th Brazilian Power Elect. Conf., COBEP 1999.
- [2] J. C. Giacomini, P.C. Cortizo, P. F. D. Garcia, and W. S. Lacerda, "Two switching DC power supplies with high power factor input: a comparative study", 5th Brazilian Power Elect. Conf., COBEP 1999.
- [3] R. Zane, D. Maksimovic, " Nonlinear-carrier control for high power factor rectifiers based on up-down switching converters ", IEEE Trans. on Power Elect., Vol-13, No.2, March 1998, pp. 213-221.
- [4] S. B. Han, N. S. Choi, C. T. Rim, and G. H. Cho, "Modeling and analysis of static and dynamic characteristics for buck - type three - phase PWM rectifier by circuit DQ transformation", IEEE Trans. on Power Elect., Vol-2, March 1998, pp. 323-336.

- [5] J. W. Kolar, F. C. Zach, "A novel three-phase utility interface minimizing line current harmonics of high-power telecommunication rectifier modules", *IEEE Trans. on Ind. Elect.*, Vol-44, No.2, August 1997, pp.456-467.
- [6] F. P. De Souza, I. Barbi, "A unity power factor buck pre-regulator with feedforward of the output inductor current", *IEEE APEC Record* 1999, pp. 1130-1135.
- [7] M. L. Heldwein, A. F. De Souza, and I. Barbi, "A simple control strategy applied to three-phase rectifier units for telecommunication applications using single-phase rectifier modules", *IEEE PESC Record* 1999, pp. 795-800.
- [8] J. G. Cho, J. W. Back, D. W. Yoo, and H. S. Lee, "Reduced conduction loss zero-voltage-transition power factor correction converter with low cost", *IEEE Trans. on Ind. Elect.*, Vol-45, No.3, June 1998, pp. 395-400.
- [9] I. R. Barbosa, J. B. Vicira, J. A. Lambert, L. C. de Freltas, and V. J. Farias, "A family of PWM soft-single-switch converters without voltage and high current stress", *5th Brazilian Power Elect. Conf., COBEP* 1999.
- [10] F. T. Wakabayashi, C. A. Canesin, "A new HPF-ZCS-PWM boost rectifier", *5th Brazilian Power Elect. Conf., COBEP* 1999.
- [11] C. M. C. Duarte, I. Barbi, "A family of ZVS-PWM active clamping DC/DC converters featuring soft commutation in both active and passive switch", *5th Brazilian Power Elect. Conf., COBEP* 1999.
- [12] F. C. Lee, "High frequency quasi-resonant converter technologies", *Proceedings of the IEEE*, Vol-76, No.4, April 1988, pp.377-390.
- [13] F. J. M. De Seixas, I. Barbi, "A new 12kW three phase 18-pulse high power factor AC/DC converter with regulated output voltage for rectifier units", *IEEE INTELEC Record* 1999.
- [14] P. T. Krein, "Elements of power electronics", New York, Oxford University Press, 1998, pp. 596-619.
- [15] J. L. Buchanan and P. R. Turner, "Numerical methods and analysis", McGraw-Hill, Inc. 1992, pp. 419-489 and 515-528.

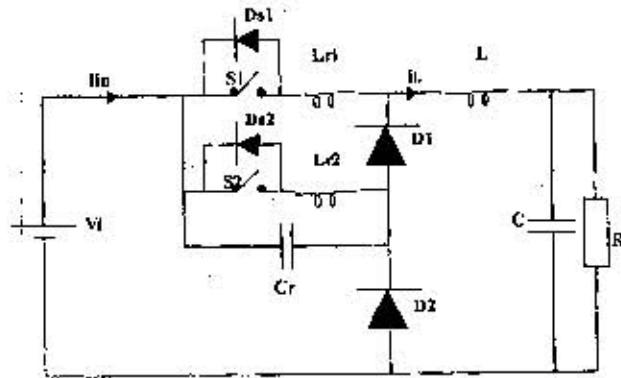
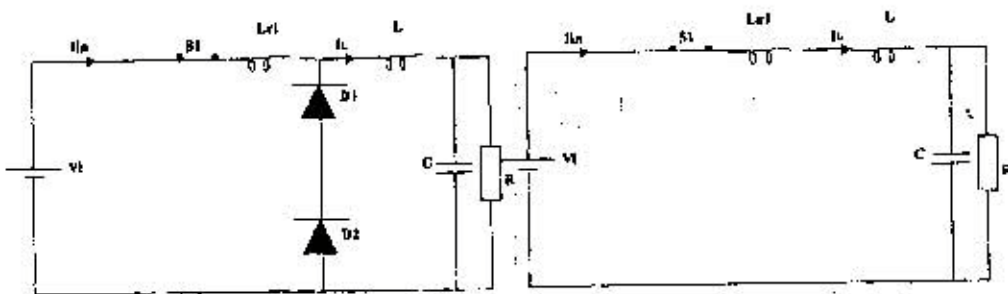
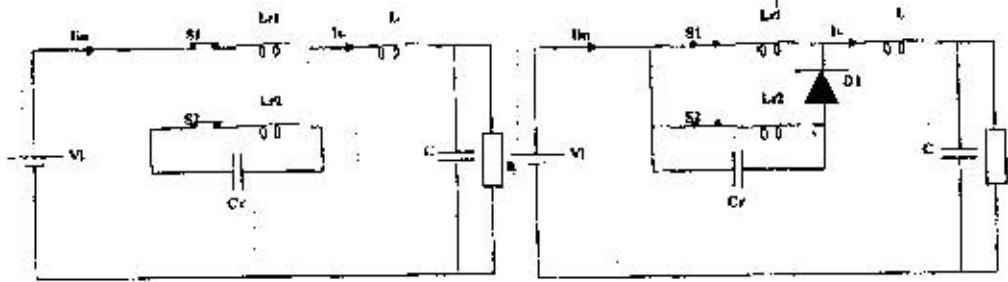


Fig.(1) Converter circuit.



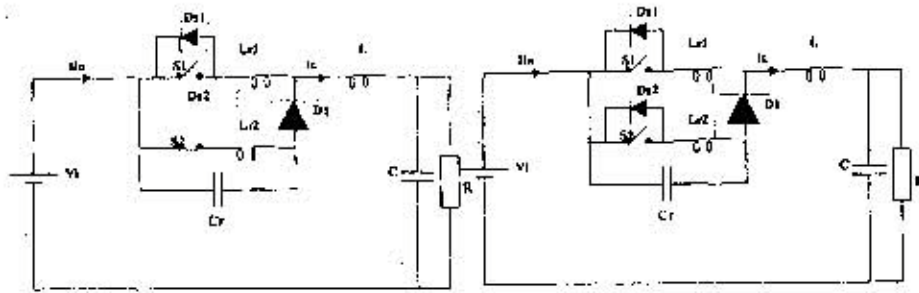
(a) Stage-1 [T0 to T1]

(b) Stage-2 [T1 to T2]



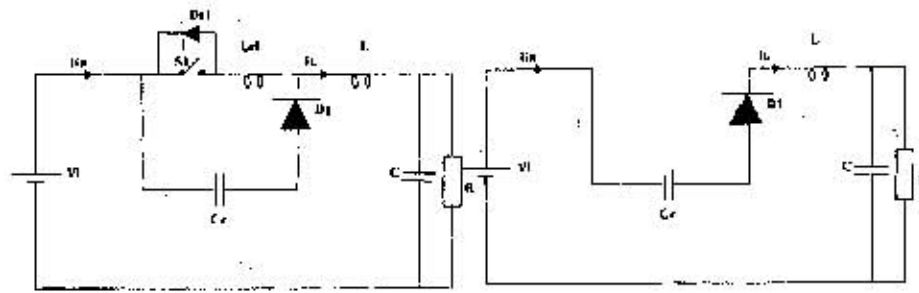
(c) Stage-3 [T2 to T3]

(d) Stage-4 [T3 to T4]



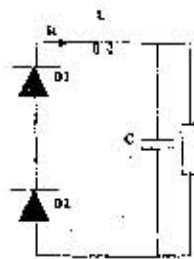
(e) Stage-5 [T4 to T5]

(f) Stage-6 [T5 to T6]



(g) Stage-7 [T6 to T7]

(h) Stage-8 [T7 to T8]



(i) Stage-9 [T8 to T9]

Fig.(2) Converter topological stages.

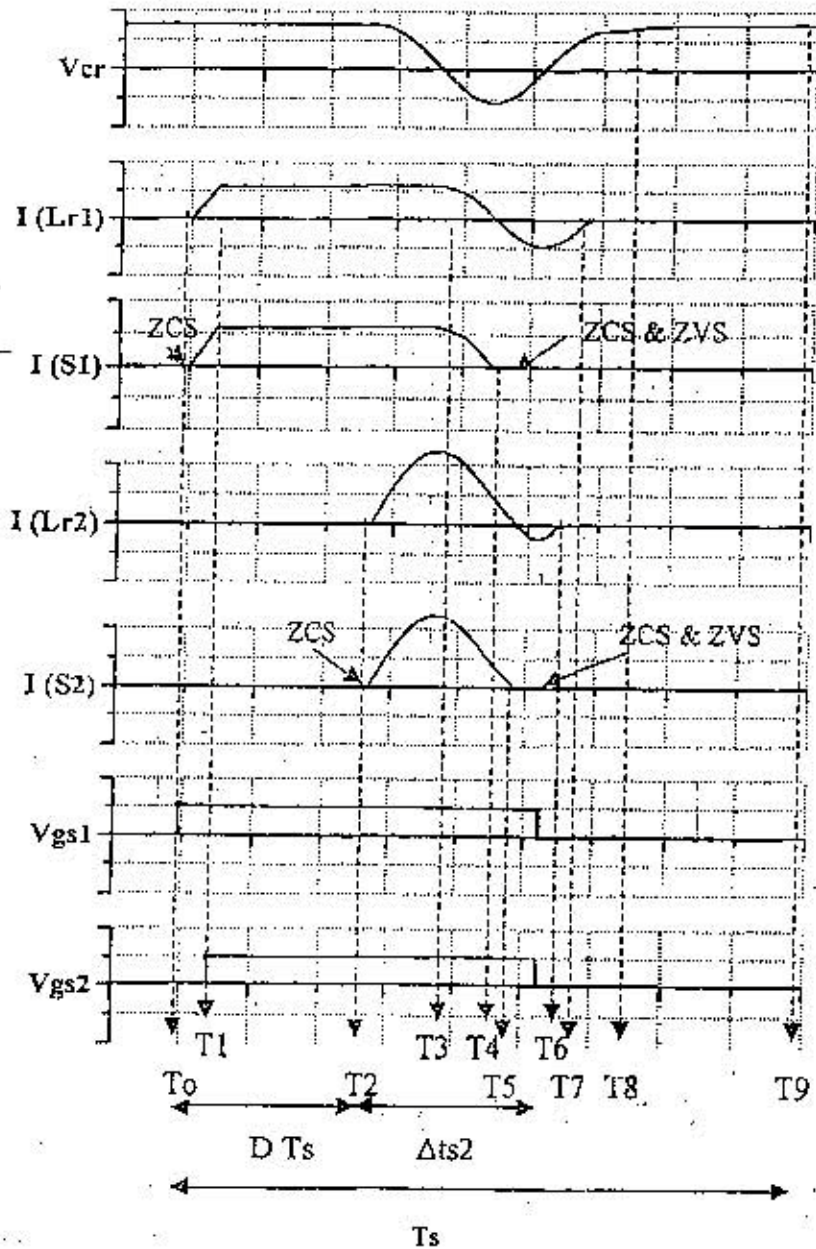
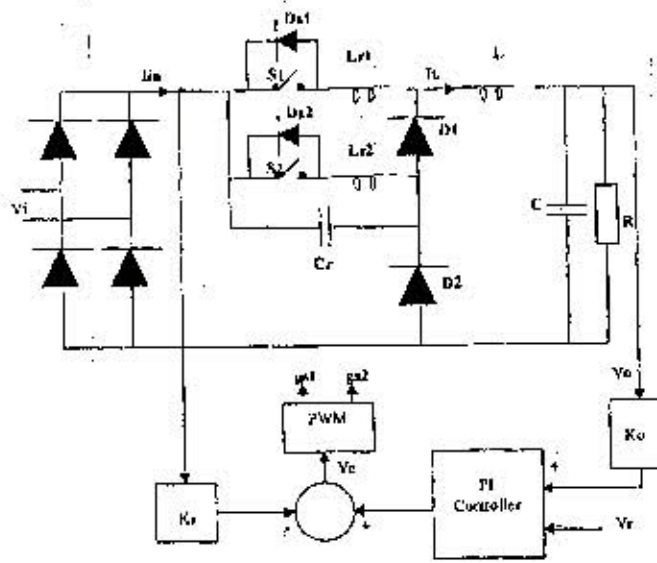
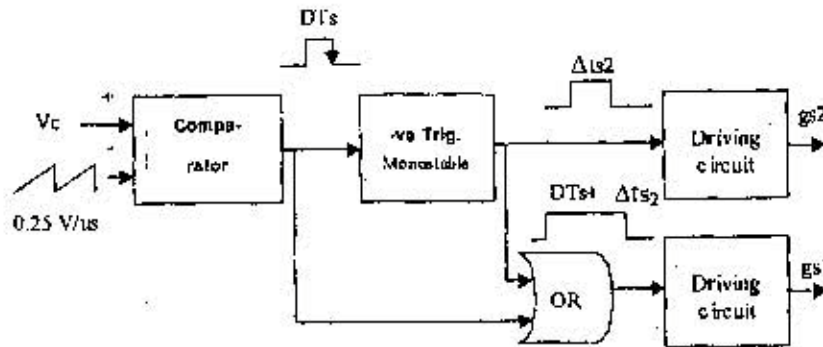


Fig.(3) Converter time diagram during one switching period ($T_s=1/F_s$).



(a)



(b)

Fig.(4) AC/DC converter system.
(a) Feedforward control system.
(b) PWM control circuit.

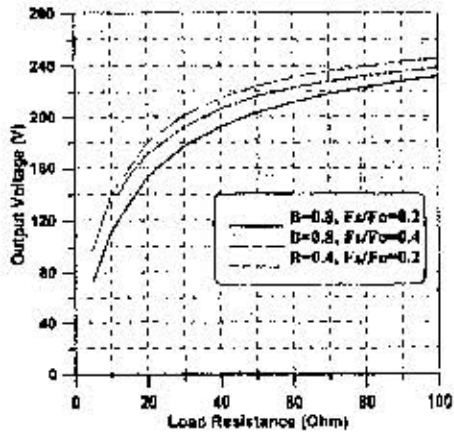


Fig.(5) Output voltage at a duty cycle ($D=0.1$) for different values of β and F_s/F_o .

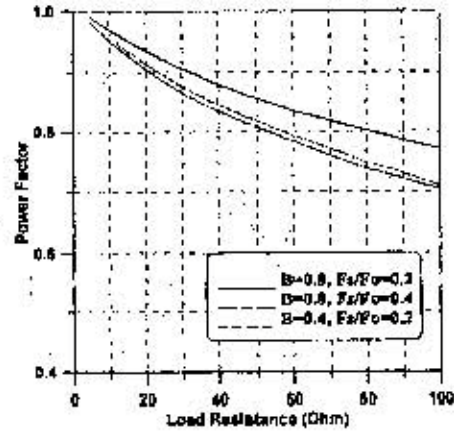


Fig.(6) Input power factor at a duty cycle ($D=0.1$) for different values of β and F_s/F_o .

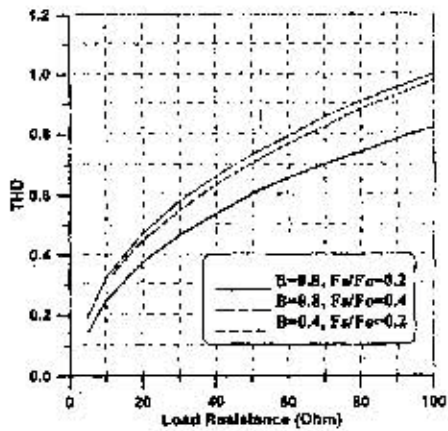


Fig.(7) Input total harmonic distortion (THD) at a duty cycle ($D=0.1$) and for different values of β and F_s/F_o .

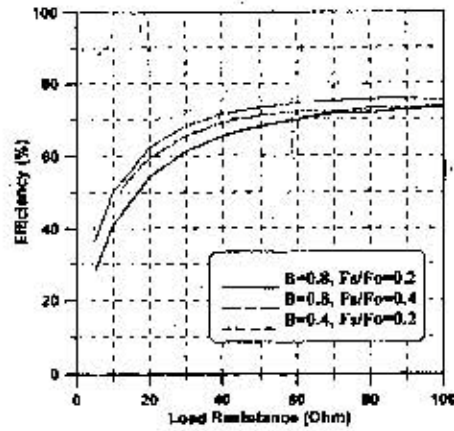


Fig.(8) Converter circuit efficiency at a duty cycle ($D=0.1$) and for different values of β and F_s/F_o .

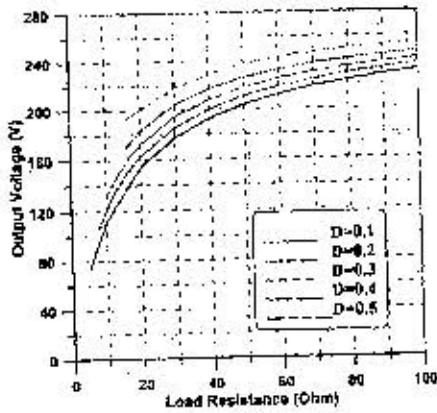


Fig.(9) Output voltage at different values of duty cycle when $\beta=0.8$ and $f_s/f_o=0.2$.

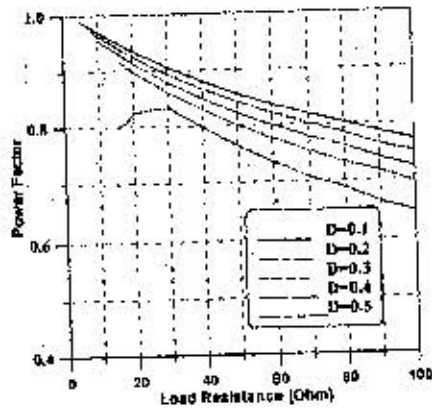


Fig.(10) Input power factor at different values of the duty cycle when $\beta=0.8$ and $f_s/f_o=0.2$.

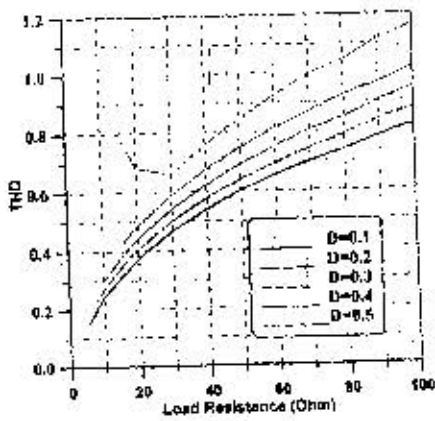


Fig.(11) Total harmonic distortion (THD) of the converter input current for different values of the duty cycle when $\beta=0.8$ and $f_s/f_o=0.2$.

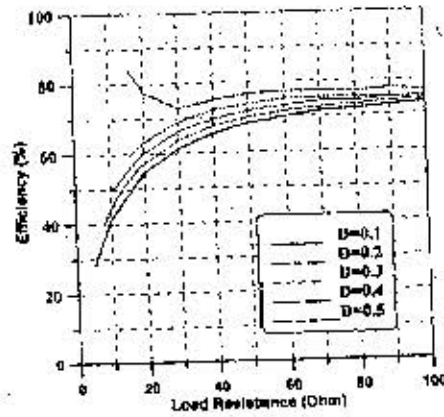


Fig.(12) Converter efficiency for different values of the duty cycle, when $\beta=0.8$ and $f_s/f_o=0.2$.

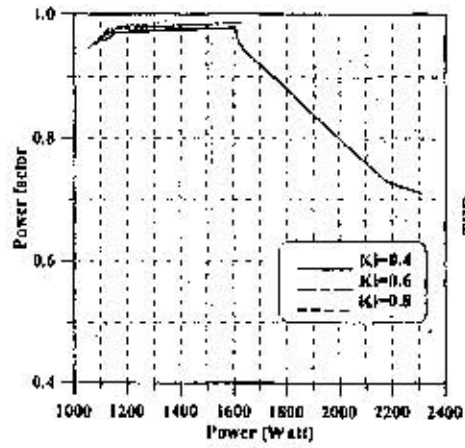


Fig.(13) Input power factor of the converter circuit with feed forward technique and at different values of K_i .

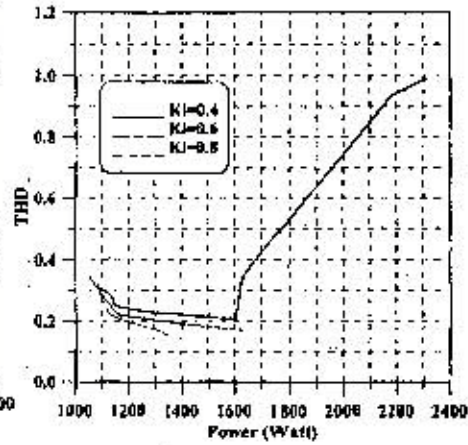


Fig.(14) Total harmonic distortion (THD) of the converter input current with feed forward technique and at different values of K_i .

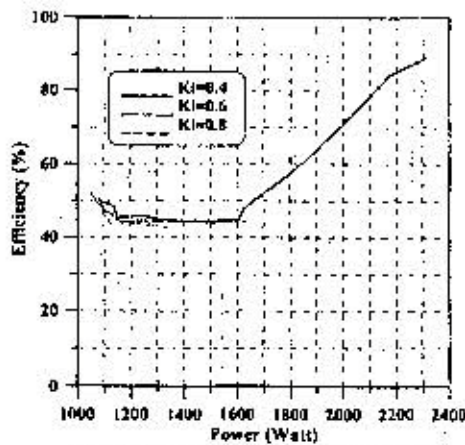


Fig.(15) Efficiency of the converter circuit with feed forward technique and at different values of K_i .

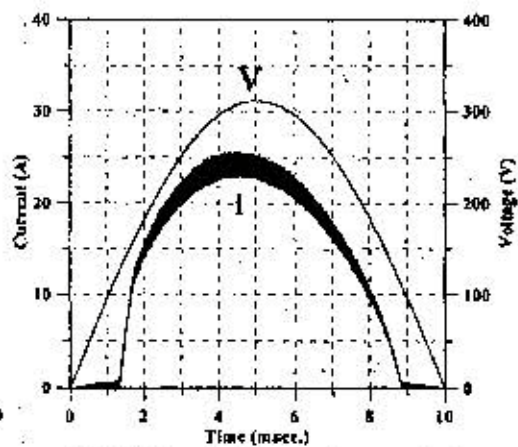


Fig.(16) Input voltage and current of the converter circuit with feed forward technique and at $K_i=0.4$.