ANALYSIS AND CONTROL DESIGN OF PARALLEL PWM DC/DC BUCK CONVERTER

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ABSTRACT

This paper presents a proposed configuration of paralleling scheme PWM DC/DC buck converter. The topological structure and operation principles are presented. A Bode plot diagram technique is used to study the stability of the scheme for different values of controller parameters and with a number of parallel modules. It is found that the results are confidence , and the proposed scheme can be used in high power applications by increasing the number of parallel modules.

تحليل وتصميم دائرة التحكم لمغير القدرة المتوازية DC/DC الخافض للجهد والمضمن بعرض النبضة

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الملخص

في هذا البحث تم اقتراح دائرة تحكم لمغير القدرة المتوازية DC/DC الخافض للجهد والمضمن بعرض النبضة مع مبدأ عمل تلك الدائرة. حيث تم استخدام تقنية مخطط بود لدراسة استقرارية المنظومة ولقيم مختلفة من معالم التحكم ولعدد المغيرات المربوطة على التوازي. إن النتائج

التي تم الحصول عليها من هذه الدائرة المقترحة كانت مقنعة بحيث يمكن استخدامه في تطبيقات القدرة العالية عن طريق زيادة عدد المغيرات المربوطة على التوازي.

LIST OF SYMBOLS

C	Smoothing capacitor, F.
D	Duty cycle.
D_1,D_2	Converter diodes.
Δd	Perturbed duty cycle value.
Δi_L	Perturbed inductor current value, A.
Δi_o	Perturbed output current value, A.
Δv_i	Perturbed input voltage value, V.
Δv_o	Perturbed output voltage value, V.
Δv_r	Perturbed reference voltage value, V.
F_s	Switching frequency, Hz.
i_L	Inductor current, A.
I_r	Reference value for the direct clipping current, A.
I_c	Common reference current, A.
K_{in}	Integral controller gain.
K_p	Proportional controller gain.
K_i	Current controller gain.
L	Converter inductor, H.
R	Load resistance, Ω.
r_c	ESR of the smoothing capacitor, Ω.
r_L	Converter inductor series resistance, Ω.
t	Instantaneous time, sec.
T_s	Total switching period time, sec.
v_c	Feed-forward signal, V.
V_i	Input voltage, V.
V_r	Input reference voltage, V.
V_o	Output voltage, V.

1- INTRODUCTION

The PWM DC/DC converter is used in many industrial applications to convert a fixed-voltage DC source into other value. Several topologies of DC/DC converters are used to step-down or step-up DC voltage. Power converters do not provide perfect regulation unless an external control scheme adjusts their operation. To perform good regulation, the duty cycle (D) of the DC/DC converter must be adjusted to cancel the effect of line variation or switch voltage drops. To achieve that a feed-forward controller in which single-loop or multi-loop controller had been suggested. The parallel DC/DC converter is used in the case of power applications. Also it has many other advantages, which can be summarized as follows:

i- Increase the capability of power processing.

ii- Improve reliability due to more even distribution of stresses.

iii- Enhance availability from the fault tolerance for the system against the failure of a single converter.

Various topologies had been introduced and studied extensively for utility and drive applications in the recent literature [1]. The designing guidelines for different topologies DC/DC parallel converters had been considered [2]. The parallel operation of DC/DC converter using 3-phase rectifier units for telecommunication application had been also achieved [3]. Stability and transient response simulation of the democratic and master slave current sharing have been discussed in [4].

In this paper, a configuration for parallel PWM DC/DC buck converter is studied. The operation and mathematical analysis are performed for the proposed topology. The stability analysis including Bode plot diagram has been presented for different controller parameters value. The Laplace transform method with numerical

method is used to analyze the response of the converter topology.

2- SYSTEM CONFIGURATION

A small-signal model of PWM DC/DC buck converter has been widely used for electronic power supplies, since it has simple construction and can be easily controlled [5]. Fig. (1) presents an open-loop DC/DC buck converter. It has a voltage source input and current source output.

The configuration of two modules PWM DC/DC buck converter, which present the proposed parallel topology is shown in Fig. (2). Each module will contain:

i- Small-signal model with pulse width modulation (PWM).
ii- Proportional and integral (PI) controller.
iii- Adder circuits.
iv- A current gain K_{ii}.

The output voltage (V_o), and the two converters currents i_{L1} and i_{L2} are feed back through a control circuit to control the switching signals. These control signals are applied to the two switching transistor in order to regulate the output voltage. The common reference current (I_c) is generated from i_L through the transfer block with gains (U_i). The gain U_i is equal to (1/n), where n is the number of parallel modules. The current error signal which is generated from comparing I_c and i_L is multiplied by gain K_i and then subtracted from the reference input voltage V_r. The output of the subtractor and the output voltage V_o are processed together by (PI) controller. The controller output is fed to the PWM circuit to produce the control pulses to the switching transistor of the converter. These processing are proceeding at the same time to all converters.

3- SYSTEM ANALYSIS

From Fig. (1), the transfer function of small-signal can be derived from the average model of the converter and by assuming that the converter is operated in continuous condition mode only, as follows [5]:

$$L\frac{d i_L(t)}{dt} = DV_i - r_L i_L(t) - v_o(t) \quad \ldots (1)$$

$$C\frac{d v_C(t)}{dt} = i_L(t) - \frac{v_o(t)}{R} \quad \ldots (2)$$

$$r_c C\frac{d v_C(t)}{dt} = v_o(t) - v_C(t) \quad \ldots (3)$$

The state variables of the average converter model can be written as a nominal value plus a small time varying perturbation as follows:

$$v_C(t) = V_C + \Delta v_C(t) ;$$
$$v_o(t) = V_o + \Delta v_o(t) ;$$
$$i_L(t) = I_L + \Delta i_L(t) ;$$
$$v_i(t) = V_i + \Delta v_i(t) ;$$
$$i_o(t) = I_o + \Delta i_o(t) \text{ ; and}$$
$$d(t) = D + \Delta d(t)$$

So equations (1), (2), and (3) can be rewrite as follows:

$$L\frac{d\Delta i_L}{dt} = D\Delta v_i + d V_i - r_L \Delta i_L(t) - \Delta v_o \quad \ldots (4)$$

$$C\frac{d\Delta v_C}{dt} = \Delta i_L(t) - \frac{\Delta v_o}{R} + \Delta i_o \quad \ldots (5)$$

$$r_c C\frac{d\Delta v_C}{dt} = \Delta v_o - \Delta v_C \quad \ldots (6)$$

Now, the transfer function for open-loop output voltage can be obtained using Laplace transforms:

$$\Delta v_o = H_1(s)\Delta v_i + H_2(s)\Delta d + H_3(s)\Delta i_o \quad \ldots (7)$$

Where

$$H_1(s) = \frac{c_5(s+c_3)D}{(s^2 + c_1 s + c_2)} \quad ;$$

$$H_2(s) = \frac{c_5(s+c_3)V_i}{(s^2 + c_1 s + c_2)} \quad ;$$

$$H_3(s) = \frac{-c_6(s+c_3)(s+c_4)}{(s^2 + c_1 s + c_2)} \quad ;$$

$c_o = L\,C\,r_c + R\,C\,L$;
$c_1 = (L + r_L r_C C + R\,C\,r_L + R\,C\,r_C)/c_o$;
$c_2 = (r_L + R)/c_o$;
$c_3 = 1/(C\,r_C)$; $c_4 = r_L / L$;
$c_5 = R\,C\,r_c/c_o$; and
$c_6 = R\,C\,r_c\,L / c_o$

The parallel topology, shown in Fig. (2), can be studied using the equations derived above for the small-single model of the converter. Bode plot diagram technique is used to analyze the stability of the topology. The following three criteria for close-loop performance are considered:
i- Open-loop transfer function G(s)H(s).
ii- Dynamic line response $\Delta v_o / \Delta v_i$.
iii- Output impedance $\Delta v_o / \Delta i_o$.

In order to analyze the parallel topology, the following assumptions are taken:
$K_{i1} = K_{i2}$; $U_1 = U_2 = U = 1/n$; and
$V_{r1} = V_{r2} = V_r$

The PI controller is presented by $(K_p + K_{in}/s)$. From equation (7), the three criteria of the closed-loop can be derived as follows:

$$G(s)H(s) = H_2(s)\,(K_p + K_{in}/s) \quad \ldots (8)$$

$$\frac{\Delta v_o}{\Delta v_i} = \frac{c_5(s+c_3)D}{(s^3 + c_7 s^2 + c_8 s + c_9)} \quad \ldots (9)$$

$$\frac{\Delta v_o}{\Delta i_o} = \frac{c_6 s(s+c_3)(s+c_4)}{(s^3 + c_7 s^2 + c_8 s + c_9)} \quad \ldots (10)$$

Where
$c_7 = c_1 + R\,C\,r_c\,V_i\,K_p / c_o$; $c_8 = c_2 + R\,C\,r_c\,V_i\,(K_{in} + K_p\,c_3)/c_o$; and $c_9 = R\,V_i\,K_{in} / c_o$

The parameters of the power stage of the converter are selected as follows [6]:

$C = 470\ \mu F$, $L = 100\ \mu H$, $V_i = 20$ V,
$r_c = 0.04\ \Omega$, $r_L = 0.04\ \Omega$, and $V_o = 10$ V

The stability of the system is detected by determined the crossover frequency and the phase margin. This can be derived from equation (8), as follows:

$$w^6 + c_{10}\,w^4 + c_{11}\,w^2 = c_{12} \quad \ldots (11)$$

Where

$c_{10} = 1/R + 1/r_c$; $c_{11} = c_3 / (R\,c_{10})$; and
$c_{12} = K_p + c_{10}\,K_{in}$

Equation (11) can be solved using Newton's method [7] to find the crossover frequency of the open-loop transfer function of the system and the resultant value of frequency will be used in equation (8) to determine the phase margin of the system.

4- RESULTS

The Bode plot diagram of the open-loop transfer function G(s)H(s) is plotted as shown in Fig. (3). It is shown that the phase margin and the cross over frequency of the system depend upon the controller parameters. The operation of the system is stable for some parameters values and unstable for other as shown clearly in Fig. (3-b and 3-c).

The dynamic line response ($\Delta v_o/\Delta v_i$) and the dynamic load behavior ($\Delta v_o/\Delta i_o$) of the system for different numbers of module n are shown in Fig. (4). It can be shown that the number of module n has little effect on the two performances.

The effect of the controller parameters values on the inductor current and output voltage waveforms are obtained as shown in Fig. (5). This figure indicates that the system is stable when K_{in}=100, but it is unstable when K_{in}=1000.

5- CONCLUSION

A parallel PWM DC/DC buck converter is proposed. The stability analysis including Bode plot diagram has been presented using a small-signal model. The simulation results indicate that the parallel scheme is stable for some controlled parameters and unstable for other parameters. It is also proved that the number of parallel module has a little effect on the stability. It is clear that the parallel scheme can be achieved for different industrial application by selecting the applicable values of the controller parameters and the number of parallel modules which are needed.

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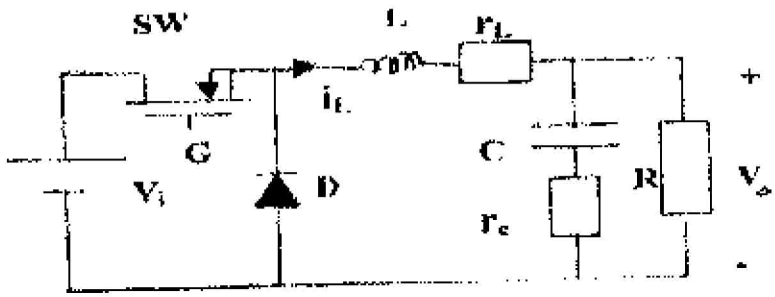


Fig. (1): Single module PWM DC/DC Converter.

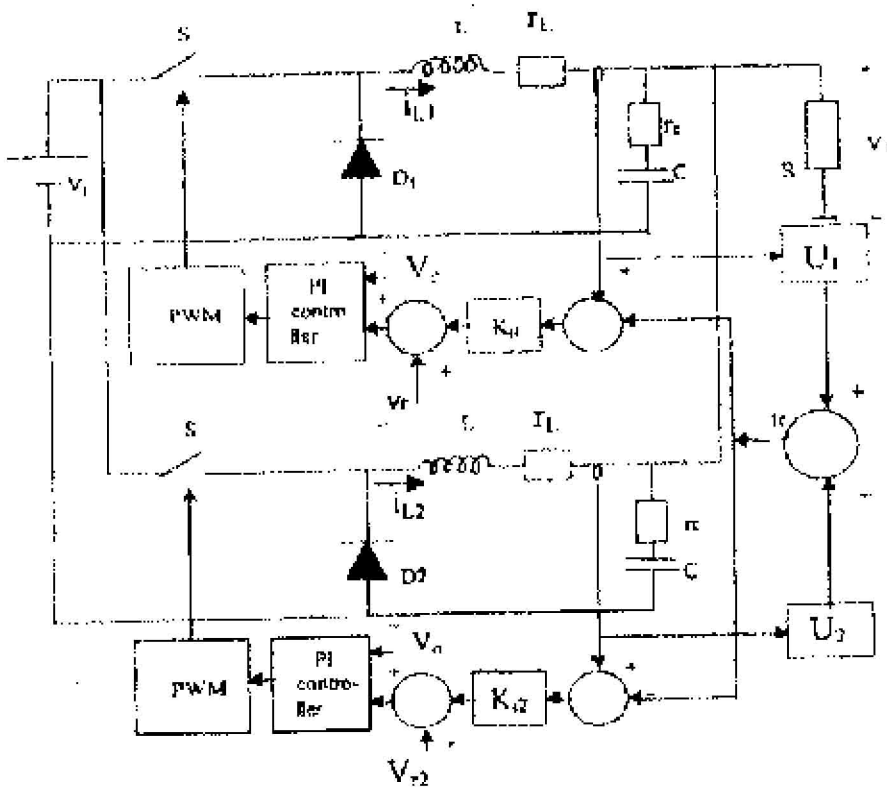


Fig. (2) : The proposed system.

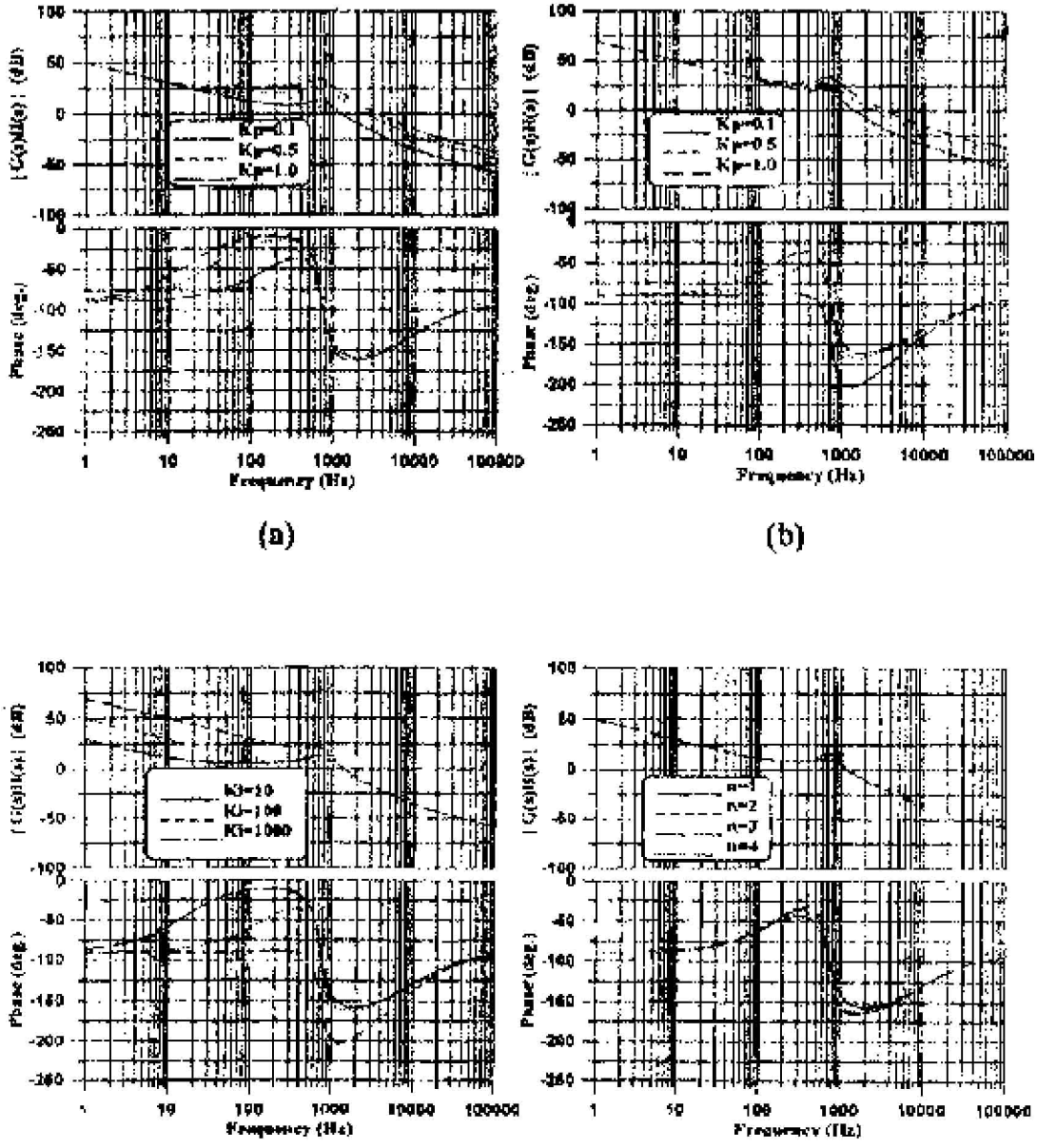
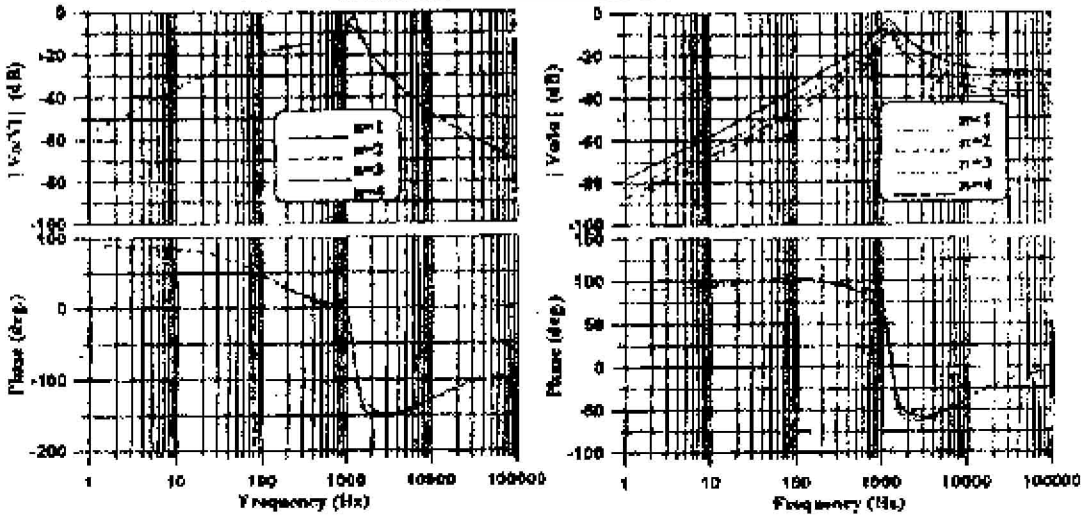


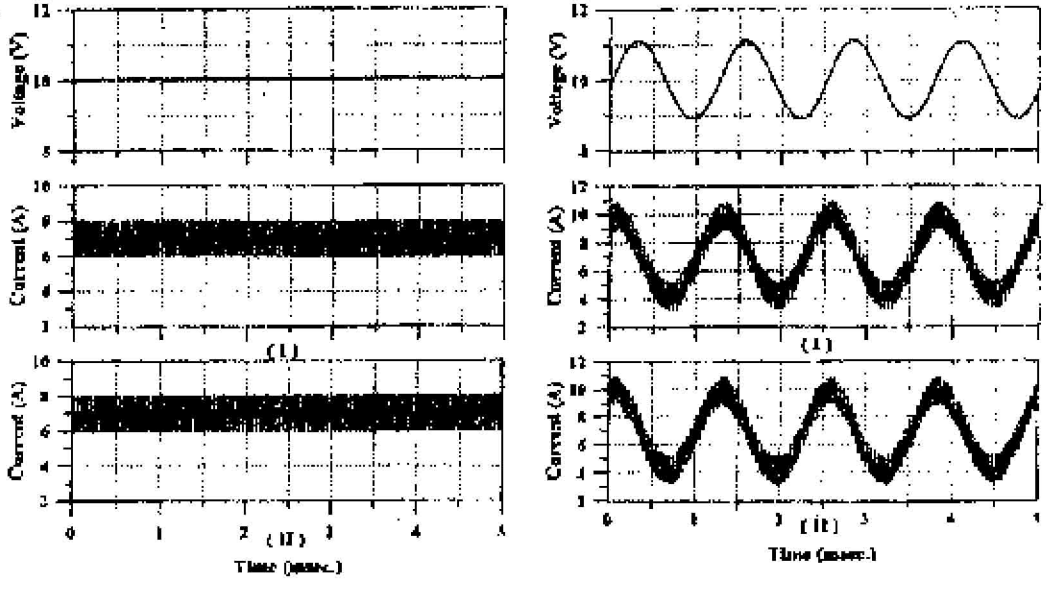
Fig. (3): Bode plots of control response when R = 1 Ω.
(i) Different values of K_p, n=2, and K_{in}=100.
(b) Different values of K_p, n=2, and K_{in}=1000.
(c) Different values of K_{in}, n=2, and K_p=0.1.

(d) Different values of n, K_p=0.1, and K_{in}=100.



(a) (b)

Fig, (4): Bode plots for different values of n with R = 1 Ω, K_p = 0.1, and K_{in} =100.(a)Dynamic line response. (b)Dynamic load behavior.



(a) (b)

Fig. (5): Inductor current and output voltage when n=2, R = 1 Ω, K_p = 0.1, K_{I1}=K_{I2}=0.1, and V_r=10 V (I) Converter 1. (II) Converter 2. (a) K_{in}= 100. (b) K_{in} =1000.