Reactive Ion Etching (RIE) for Micro and Nanogap Fabrication

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ISSN –1817 –2695

(Received 6 April 2010; Accepted 3 March 2011)

Abstract

To understand the important relationship between the biosensor and micro and nanostructures we introduce this proposal about the fabrication of micro and nanostructure by using one of the most important dry etching processes in micro and nanostructures, reactive ion etching (IC-RIE) has been applied and developed as a method for etching micro and nanogap semiconductors. PolySi material is used to fabricate micro and nanogap structure and gold as electrodes. The fabrication and preparation methods to fabricate micro and nanogaps using RIE properties are discussed along with their advantages towards the nanotechnology and biodetection. In this study, 2 masks design are proposed. The first mask is the lateral micro and nanogap and the second mask is for gold pad electrode pattern. Lateral micro and nanogaps are introduced in the fabrication process using polysilicon and gold as an electrode. Conventional photolithography and dry etching techniques are used to fabricate these micro and nanogaps based on the standard CMOS technology. As a result we need to deposit Al layer over the polysilicon semiconductor before coating a photoresist to protect the polysilicon layer during the etching (IC-RIE) for using the Al material as a hard mask. The requirement time to etch 1μm polysilicon layer completely by using IC-RIE to fabricate the micro and nanogap structure it takes approximately 40sec. These results are better than those using wet anisotropic etching techniques.

KEY WORDS: Micro &nanogap, photolithography, reactive ion etching (RIE).

INTRODUCTION

In the past two decades, the biological and medical fields have seen great advances in the development of biosensors and biochips capable of characterizing and quantifying biomolecules.
The RIE equipment used in these experiments was a Vacutech parallel-plate system. The lower electrode is powered by a 13.56 MHz-RF generator coupled through an automatic tuning network. Each electrode is 200 mm in diameter and the distance between them is 23 mm. The RF electrodes are made of anodised aluminium. The chamber volume is 131 and the system is pumped by a 350 l/rain lurbomolecular pump backed by a mechanical rotary vane pump. The base pressure before each run was less than 5 x 10^{-2} Torr. A two-level factorial design of experiments was used to find the main and interaction effects governing etch rate and sidewall slope. Even through the RIE process performance is influenced by the interaction effects between different factors, such as, oxygen content, power density, pressure and loading, at a chosen set of etching parameters.

Different techniques and schemes such as, sandblasting, mechanical grooving, and wet

chemical etch; laser sculpturing and plasma etching have been used to texture the surface of single and polycrystalline silicon. One of the characteristics of all these methods is that they use either chemical- or physical-etching mechanisms to produce the desired pattern. This imposes limitations such as features geometry or selectivity of the process depending on which mechanism is chosen [1].

In recent years, nano-ordered materials have attracted much attention since the products have been smaller in keeping with a trend of density growth or integration in various technology fields. They have great interest because of their potential to exhibit novel properties which cannot be achieved by bulk materials. For example, two-dimension (2D) and three-dimensionally (3D) ordered materials have attracted much interest due to their potential applications in photonic crystals [2–5], data storage [6–9], field emission device [10–13]. It is necessary to establish the fabrication techniques of materials with desired shape or size depending on each application. For example, they must have periodic pillar or hole structures with high aspect ratio to use as 2D photonic crystals [11, 12]. It is necessary to be moth eye structure for use as antireflection coating [13, 14], which has pointed top preferably for field emission device [15].

Micromachining in silicon is widely employed for the fabrication of various micromechanical structures needed for many types of sensors and actuators Pattern transfer based on various etching processes it plays an essential role in micromachining in the development of etching processes for micromachining. It is important to maintain high etch rate, good control of line width, good uniformity and high selectivity over both masks and underlying layer. However, most of the traditional wet etchants are unable to meet these requirements for several reasons. First, there is pure chemical reaction involved in the wet etching, resulting in an isotropic etching profile unless a crystal orientation dependent etch is used. Secondly, the adhesion of photoresist to the substrate is often poor due to the attack of the etchant. Thirdly, the surface tension of the liquid makes it impossible for the wet etchant to penetrate through very small windows in resist pattern and react with substrate. Fourthly, gas bubble formation during the etching locally prevents the etching from proceeding and leads to poor uniformity although some of the wet etchants for bulk micromachining, such as KOH or EDP, etch crystal silicon anisotropically, their etching characteristics strongly depend on the crystal orientation, doping concentration and electrical potential of the substrate. As a result, the type, shape and size of the structures that can be realized are limited [16].

In previous reports, a variety of techniques for narrow nanogap fabrication has been demonstrated: electron beam lithography [17], [18], electromigration [19], mechanical break junction [20], sacrificial layer-assisted silicon and gold nanogaps [21], and surface-catalyzed chemical deposition [22]. However, except for electron beam lithography and sacrificial layer-assisted nanogaps, all other techniques have several problems in nanogap commercialization because of the complex steps and difficulties in fabricating reproducible nanogaps and their compatibility with other semiconductor circuits and processes. Therefore, new approaches and integration [23] methods for fabricating nanogap arrays need to be developed in order to overcome these problems.

On the other hand metallic nanoparticles have been used to establish self-assembly nanostructure of which physical and chemical properties have been investigated in recent years. In particular, gold nanoparticles can be easily prepared and have the characteristic of biocompatibility. Some new devices have been developed for the application of immunoassay by making use of the novel properties of nanostructure that is self-assembled by gold nanoparticles [24]. However, the properties of gold nanostructure can vary significantly with the size of gold nanoparticles and the pitch between gold nanoparticles in the nanostructures [24–26]. A gold-amplified sandwich immunoassay for the detection of human immunoglobulin G has also been developed by Natan and coworkers [26]. The sensitivity of their immunoassay can reach 1 pM. They have also conducted a series of studies on the effect of particle size and surface coverage on the detective sensitivity of immunoassay [27, 28].

A gap in a material with a high magnetic permeability causes magnetic field lines to leak into the surrounding ambient environment (air). If this gap is varied in size, the density of the field at a given point in that area will change.

MEMS fabrication techniques enable the design and fabrication of a device that can take advantage of this behavior and locally modulate a static magnetic field [29].

METHODOLOGY

In this research, SOI wafer is used to fabricate a micro and nanogap biosensor. The first step is to design and produce a mask, which is two mask designs are proposed, the polysilicon micro and nanogap with gold electrode process flow are develops. This research is mainly focusing on the issue related to the fabrication of the micro and nanogap and the development of a new technology. The sidewall etching using IC-RIE to form thin micro and nanogap metal cantilevers which configured the 3-D micro and nanogap electrode grid array structure. Anisotropy of RIE is modeled and the etching profiles are simulated.

The starting material used in this research is a P-type, 100 mm in diameter (4 inch wafer) silicon-on-insulator (SOI) wafer as shown in figure 1.

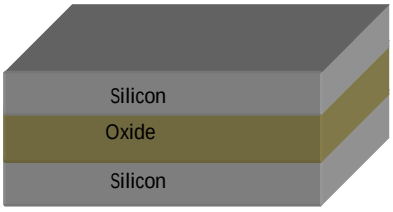


Figure 1: SOI Wafer

Silicon on insulator (SOI) wafers are used to reduce parasitic device capacitance and thus improve the final device performance.

The first process is to check the wafer type from its specification, measure wafer thickness (SOI thickness), measure the sheet resistance. After that, lightly scribe the backside of each wafer, protect the top surface, using the scribe tool provided. Mark gently but make it visible and place scribed wafer in container.Wafer is cleaned before each process.

As for the lithography process, two photomasks are employed to fabricate the micro and nanogap using conventional photolithography and polysilicon etching techniques. Commerical chrome mask is used in this research for better photomasking process. This mask is used to develop the gold electrode with polysilicon micro and nanogap. The photomasks are designed using AutoCAD and then printed onto a chrome glass surface.

Figure 2 shows the first mask for micro and nanogap electrode formation which is the length and the width of 5000µm and 2500µm respectively.

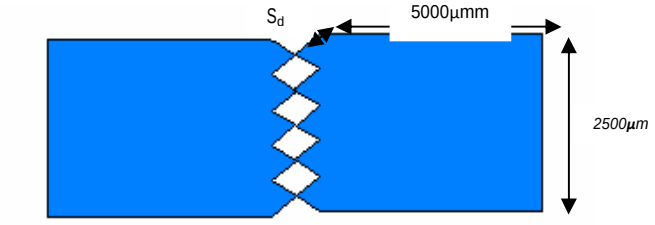


Figure 2: Design specification of the first Mask.

The proposed angle length of the end electrode is shown in table 1. This is simply to check the best angle for the best micro and nanogap formation after etching process.

Table 1: Difference dimensions for S_d.

S_d	1	2	3	4	5	6
μm	600	700	800	900	1000	1100

The symbol S_d refers to the dimension for side angle of the design for micro and nanogap formation. It shows that when S_d is large, it means that the micro and nanogap become very sharp and less sharp with less dimension of S_d.

Figure 3 shows the actual arrangement of device design on chrome mask. It consists of 160 dies with 6 different designs.

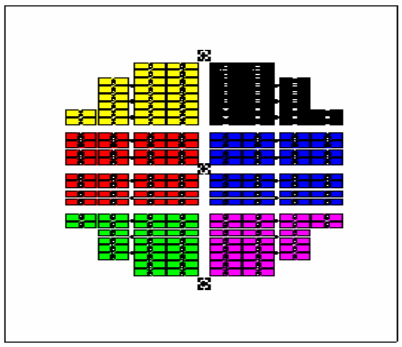


Figure 3: Schematic nanogap design of the actual mask1on chrome glass

Figure 4 shows a schematic device design of mask 2 with 5000μm length and 2500μm width. The distance between two rectangles indicated as S_a bearing the same dimension with S_d according to the theory of Pythagoras, and the dimension of S_a can be defined mathematically as shown in figure 5.

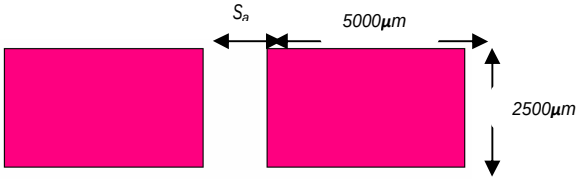


Figure 4: Design Specification for Mask2

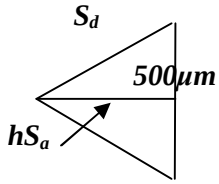


Figure 5: Schematic representation S_a, where $S_a=2hS_a$

Table 2: Variance Dimensions for S_a and S_d

S_d (μm)	600	700	800	900	1000	1100
$hS_a=((S_d)^2-(250)^2)^{½}$ (μm)	545	653	759	864	968	1071
$S_a=2\ hS_a$ (μm)	1090	1307	1516	1729	1963	2139

From the above table the dimension for S_a depends on the dimension of S_d. The calculated S_a is based on $S_a=2hS_a$

Figure 6 shows a schematic mask on chrome glass

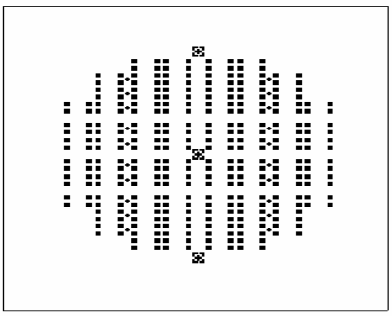


Figure 6: Schematic electrode Mask 2 on chrome glass

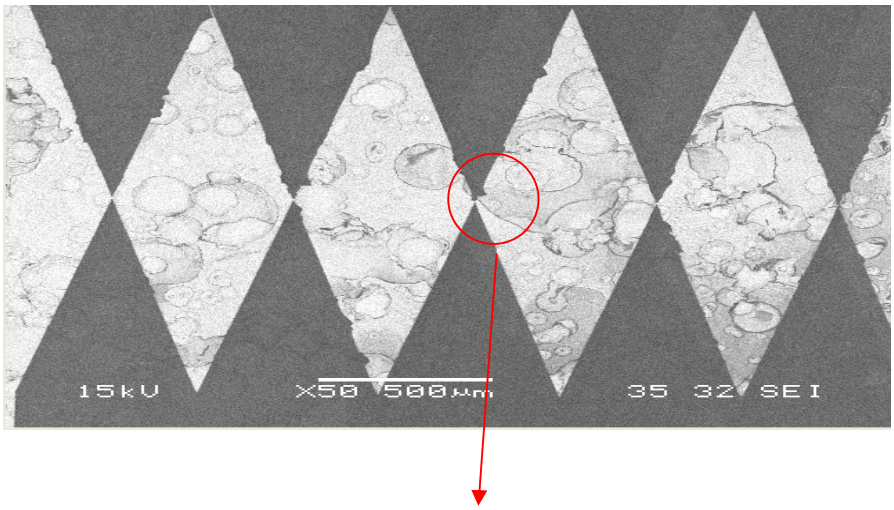
RESULTS AND DESCUSSIONS

The proposed process steps of gold electrode with polysilicon micro and nanogap fabrication are shown in figure 7. After cleaning the SOI wafer, deposit 600nm polysilicon layer over the SOI wafer before applying photolithography process, a layer of positive photoresist is first coating the SOI surface, and then exposed to ultraviolet light through a mask 1. After development only the unexposed resist will remain. After that, apply dry etching process for polysilicon layer to confirm the micro and nanogap for the micro and nanostructure using the recipe's parameters as explained in table 3.

Table 3: Polysilicon dry etching process recipe.

Cf_4	CHF_3	SF_6	O_2	Ar	Bais	Power ICP power	APC/control(Pa)	Etching Time
0	0	50	0	30	250	650	4.00	24 sec

After removing the resist we can show by using SEM some damage in the photoresist layer for the pattern as shown in figure 8.



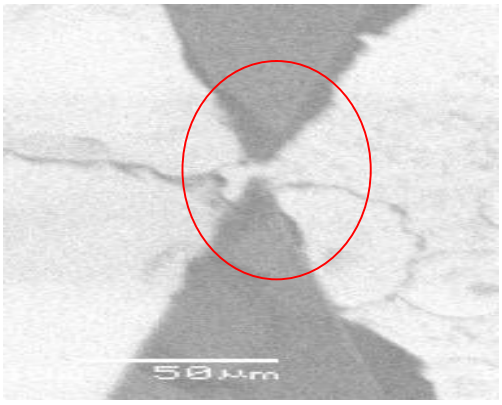


Figure 7: SEM photo for polySi microgap after using dry etching RIE

It is clearly shown that there is a problem in the gap pattern, this affects negatively on the results of the examination for the electrical device characterization, and the proposed is depositing 140nm Al layer as a hard mask to avoid the damage of the polysilicon layer during etching process by using the RIE. Next, in the photolithography process, a layer of positive photoresist is first applied to the Al surface, and then exposed to ultraviolet light through a mask 1. After development only the unexposed resist will remain. As in figure 10(d) a wet etching process of AL layer is performed before removing the resist. After that, apply dry etching process for polysilicon layer by using the same recipes parameters in table 3 to fabricate the micro and nanogap for the micro and nano structure, then apply wet etching to remove the Al layer, and figure 9 shows SEM image after applying dry RIE for the polysilicon pattern.

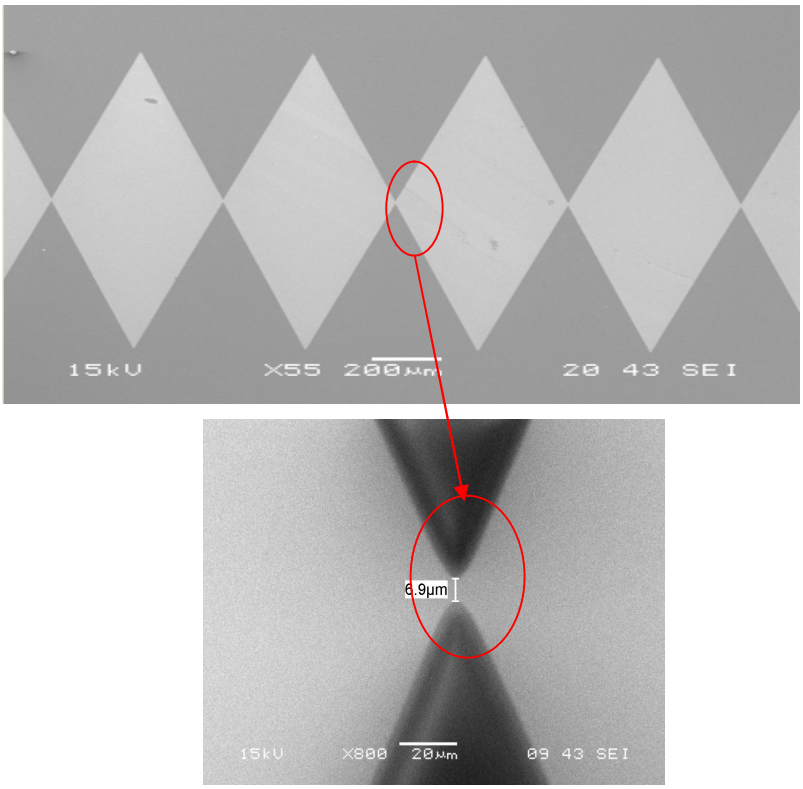


Figure 8: SEM image after dry etching for Polysilicon micro and nangap structure

It is clearly shown that the change that took place in the polysilicon design after the deposition of the Al layer as a hard mask and how it has become sharper, and of course these positive results in the etching process lead to good results in the biodetection process because the RIE is an essential process in the micro and nano fabrication. Figure 9 shows the planned

amount of fish and supply which was etching in the RIE process.

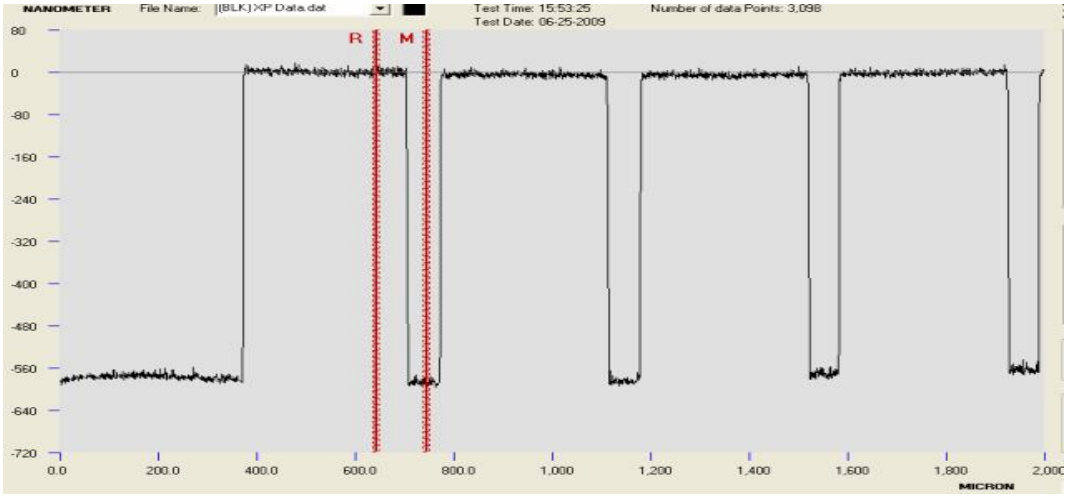


Figure 9: the thickness measurements for polysilicon pattern after dry etching process.

The figure(9) clears that the RIE process is applied to more than 550nm of the PolySi layer thickness and display the shape engraved up to 2000ìm. After fabricating the gap, we proceed to fabricate the gold electrode where deposit a layer of 30nm/100nm for Ti/Au substrate as a first step to design the electrode, following the resist coating process. After exposing mask2 the layer of the resist is developed, then wet etching process of Ti/Au substrate is performed before removing the resist. Finally a structure of the gold electrode with polysilicon micro and nanogap is obtained as shown in figure 10(g).

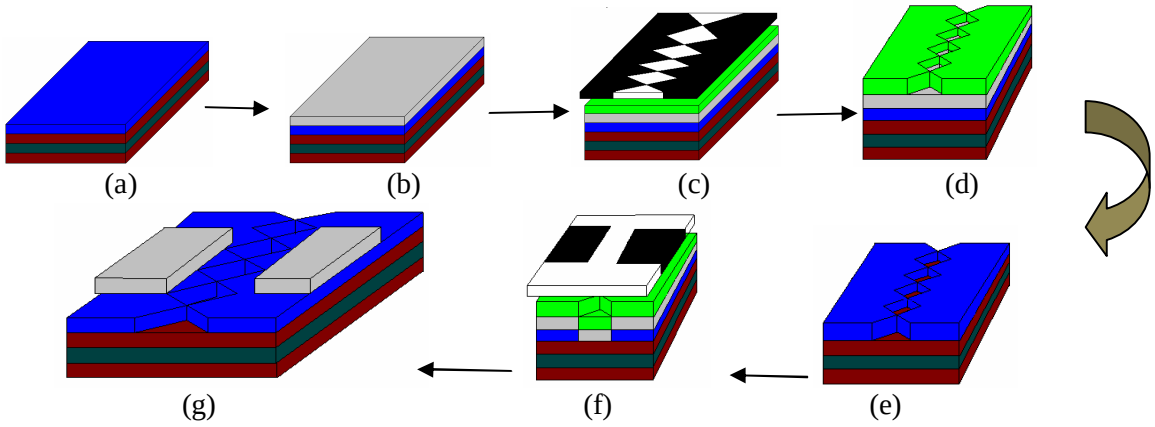


Figure 10: Al/ PolySilicon- Silicon oxide structure process flow

An important issue in device fabrication is the ability to remove dry etch induced-damage in order to restore the electronic properties of the material.

Really, the patterned Al was acted as a hard mask for protecting the polysilicon layer during the etching process. Laterally etch rate is obtained by the measuring of image sizes difference between before and after etching with using SEM. In addition, the whole etching processes were done using ICP reactive ion etching system with etching parameters of basic recipe as shown in Table 3 which then was further developed to control the nanostructure dimension.

Etch process needs a perfect result of just one step of nanopatterns development, since stepped image development can lead to contaminations and then many porosities and un-etched areas result. On the other hand, resist patterns that

were developed for sufficiently long time led to resist patterns that were removed of adjusted positions and they were even frequently solved in developer solution. However, optimum development time depends strongly on many parameters such as usage age of developer, resist thickness, soft bake time and density of patterns. In addition, higher patterns density led to longer development and etching times.

From the observation of the experiment, the RIE mechanism is assumed to consist of both chemical and physical reaction in the chemical reaction, radicals as active gas molecules react with PolySi molecules and reacted formations are removed, consequently, the process becomes isotropic. Furthermore, this chemical reaction is activated by an impact of ions, that is, a kind of ion sputtering effect. This additive action is physical and has a directional characteristic owing to an incident angle of ions, usually perpendicular to the electrodes (vertical). Under a certain etching condition, both the chemical and the physical reaction take place simultaneously, therefore, the etched shape may be decided by the ratio of each etch rate that can be defined as an instantaneous etch factor

CONCLUSION

ICP-RIE has been developed successfully as a method to etch polysilicon in a homogeneous way, independently of the grain orientation on the surface. PolySi micro and nanogap structure was produced and fabricated in this work. The etching rate measurements explain the stripping 1μm take 40sec for bolySi material. These results are better than those using wet anisotropic etch techniques. The fabrication and development of micro and nanogap structure by using reactive ion etching (RIE) process need to deposit Al layer as a hard mask to avoid the damage during the etching.

ACKNOWLEDGMENT: We are grateful for fruitful discussions with our collaborators at the Institute of Nano Electronic Engineering (INEE) on the University Malaysia Perlis (UniMAP). This work was supported by (INEE) at (UniMAP), through the nano technology project. The views expressed in this publication are those of the authors and do not necessarily reflect the official view of the funding agencies on the subject.

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تقنية الحفر الجاف في تصنيع المايكرو (نانو) فجوة

الملخص :

في العقدين الماضيين احتلت مجالات البايولوجي والطب اهميه عظيمه في تطوير علوم حساسية البايو ورقائقه عــن طريــق تشخيص وتحديد نوع جزيئاتها.

لفهم العلاقه الوطيده والمهمه مابين علم حساسية البايو وعلم تصنيع اجهزه بتقنية النانو والمايكرومتر، اعددنا هذا البحث في تصنيع جهاز بقياسات المايكرو (النانومتر) باستخدام واحده من العمليات المهمه في هذا المجال وهي تقنية الحفر الجاف باستخدام جهــاز الحفر الفعال حيث طور الاخير وحددت البارامترات المستخدمه فيه لتتم عملية الحفر بصورة دقيقة وعلى احسن وجه.

بولي سيليكون هي المادة المستخدمة في عملية تصنيع تركيب المايكرو (نانو) فجوة ، والذهب في عملية تصنيع الاقطاب. عمليــة التصنيع والطرق التحضير في هذا العمل نوقشت بتسلسل دقيق في فقرة النتائج والمناقشة.

في هذه الدراسة تم اقتراح ماسكين اثنين حيث يستخدم الاول في تصنيع تركيب المايكر (نانو) فجوة الافقيه، والاخر في تــصنيع الاقطاب الذهبيه للجهاز.

مبدئي الفوتوليثوغرافي والحفر الجاف يستخدمان في تصنيع التركيب اعلاة مبني على اساس تقنية .CMOS

كنتيجه، نحتاج لترسيب طبقة من الالمنيوم فوق طبقة البولي سيليكون لحماية الاخير اثناء عملية الحفر الجاف باستخدام ، وبالتالي تستخدم الالمنيوم كطبقة حماية لتركيب البولي سيليكون. IC-RIE

ان الوقت المطلوب لحفر من طبقة البولي سيليكون تماما باستخدام لتصنيع جهاز المايكرو (نانو) فجوة تقريبا يحتاج الــى زمــن مقدارة ، حيث ان هذه النتائج هي افظل بكثير فيما لو استخدمت عملية الحفر الرطب بدلا من تقنية الحفر الجــاف40 Sec -IC µ1m RIE