

Electrical and Electronical Properties of Silicon Nanostructure Produced by Electronical Etching

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Abstract

Porous silicon constituting silicon nanostructures layer have been produce on crystal silicon using different preparation condition in electronical etching process. The electrical properties of the PS/c-Si heterojunction were studied and adopted to obtain the electronic structure and construct the energy band diagram of the device. This device could be used in various applications and was found to be a staggered type.

الخصائص الكهربائية والإلكترونية للسليكون ذو التركيب النانوي المحظر باستخدام طريقة التتميش الكيميائي

الخلاصة

في هذا البحث، تم تحضير السليكون المسامي مشتملا على السلكون ذو التركيب النانوي على بلوره سليكون باستخدام شروط تحضير مختلفة. حيث تم استخدام تقنية التتميش الكهروكيميائي من اجل تحضير طبقة السليكون المسامي، الازم من اجل الحصول على المفرق الهجيني نوع (Ps/Si). تم قياس الخصائص الالكترونية ووجدت لتكون معتمدا على مقدار تيار التكوين وتم تحديد مخطط الطاقة للنبيطة المحظرة. ان هذه النبيطة يمكن ان تستخدم في مختلف التطبيقات ووجد ليكون من النوع الحاد.

Introduction

Heterojunction devices have been drawn a great attention in recent years mainly due to their use in optoelectronic field [1]. The properties of these heterojunction are of very importance when they are used as FET, bipolar transistor, light emitting diode and lasers[2]

The heterostructure PS/p-Si is considered as anisotype heterojunction since PS behaves like n-type semiconductor. The junction capacitance (C) of the anisotype heterojunction of abrupt type can be expressed as [3]:

$$C = \left[\frac{q e_1 e_2 N_A N_D}{2(e_1 N_A + e_2 N_D)} \right]^{1/2} (V_{bi} - V_a)^{-1/2} \quad \dots(1)$$

where ϵ_1 and ϵ_2 are permittivity of narrow bandgap and wide band gap respectively, N_A and N_D are

respectively the free carrier concentration of p-type and n-type semiconductors and V_a is the applied voltage.

Current Transport Mechanism of such Heterojunction could be explained According to any of the diffusion model, the emission model, and the recombination model [4,5,6], a relation between J and V is represented by:

$$J \propto \exp\left(\frac{qV}{\eta kT}\right) \quad \dots\dots(2)$$

where q/kT is the reciprocal of volt equivalent of temperature and η is the diode factor.

The aim of this work is to obtain the electronic structure of the Ps/Si heterojunction and study the

optoelectronic properties of the device.

Experimental details and measurements

A commercially available P-Si of square-shaped samples each of 1x2cm² area, of two different resistivity of (2.179, 0.0037)ohm.cm were prepared using a wire-cut machine. Those samples were etched with CP4 solution consisting of (HNO₃, CH₃COOH, HF) of ratios (3:3:5) to remove oxides. Then they were cleaned with alcohol and ultrasonic waves produced by Cerry PUL 125 device for 15 minutes then cleaned with water and ultrasonic waves for 15 minutes. Ohmic contacts were fabricated by evaporating 99.999 purity aluminum wires using Edwards coating system. The resistivity and type of conductivity of the Si substrates were measured by using (FPP) technique. Ps samples have been produced by the electrochemical etching process. The samples has been prepared at two different current density of 40 , 60 mAmp/cm² Ohmic contacts were made on both, Ps and c-Si by deposition Al film respectively , After contact and assembly processes I-V characteristic under different operating temperatures for both sample. C-V characteristics of the produced heterojunction were measured using a PM6306 programmable LRC meter supplied by Fluke at 10 KHz and reverse bias voltage ranged from (0.5-5) V. The cross point (1/C²=0) of the (1/C²-V) curve represents the built-in potential (Vbi) of the heterojunction [7] , The depletion layer width has been estimated using the following equation:

$$W = \sqrt{\frac{2 e_s v_{bi}}{q N_s}} \dots(3)$$

The energy band diagram of PS/c-Si heterojunction has been made theoretically depending on the experimental results , which are used in the analysis of the capacitance-voltage characteristics, photocurrent spectra, current - voltage characteristics and their temperature dependences. The Fermi level energy has been found according to the following equation :

$$E_c - E_{fn} = \frac{kT}{q} \ln\left(\frac{N_c}{N_d}\right) \dots(4)$$

$$E_{fp} - E_v = \frac{kT}{q} \ln\left(\frac{N_v}{N_a}\right)$$

The difference between the two conduction band energies is denoted by ΔEc and the difference between the two valance band energies is denoted by ΔEv.

$$\Delta E_c = E_{cn} - E_{cp} \dots(5)$$

$$\Delta E_v = (E_{gn} - E_{gp}) - (E_{fn} - E_{fp}) \dots(6)$$

and

$$\Delta E_c - \Delta E_v = E_{gn} - E_{gp} = \Delta E_g \dots(7)$$

E_{gn} and E_{gp} are the energy of wide band and narrow gap material respectivity. On the other hand, current mechanism employs the emission model and it value given in the following equation[4]:

$$I = A \exp\left[\frac{-q(\Delta E_c - V_{bi})}{KT}\right] \left[\exp\left(\frac{qV}{KT}\right) - 1\right] \dots(8)$$

where V is the applied bias ,and x₁ < x₂ < x₁+E_{g1} and φ₁ > φ Where x₁ , x₂ is the electron affinity for the two semiconductor materials

Result and discussion

C-V characteristic of heterojunction is shown in Figure (1), which is one of the most important measurements since it determines different parameters such as built-in potential, junction capacitance and junction type. The following figures give the C-V and $1/C^2$ -V measurements for both junctions at optimum etching current density. This result shows that the junction capacitance is inversely proportional to the bias voltage for all prepared samples. The C-V characteristics of the prepared device depends on the morphology and the porosity of the etched Si surface. It is clear from the same figure that the values of junction capacitance were increased with the substrate resistivities, this is related to the same reason by which the resistivity affects the prepared junction.

The reduction in the junction capacitance with increasing the bias voltage results from the expansion of depletion layer with the built-in potential. The depletion layer capacitance refers to the increment in the charge per unit area to the incremental change of the applied voltage. This property gives an indication of the behavior of the charge transition from the donor to the acceptor region, which was found to be “**abrupt**”, this means that the depletion layer is constant and hence the carrier concentration will be constant at the depletion layer given in Figure (1) in which the etched surfaces contains a pore-like structures. A linear relationship between C^{-2} and reverse bias voltage was obtained for the

structures. This linear relationship represents the heterojunction between the PS layer and c-Si. The value of the built-in potentials for both substrate resistivity and different etching current density for the prepared junction has been obtained and it has been found to have different values depending on the properties of the prepared device since it represents the energy required by the electron to transfer from the c-Si to PS. The value of V_{bi} is expected to depend on the Fermi level position in the conduction band at high carrier concentrations.

The relative permittivity (ϵ_{psi}) of the PS layer is determined from the C-V characteristics at the zero reverse bias voltage and the related result is given in table (1) for both resistivities respectively with different etching current density. It is clear that the relative permittivity (ϵ_{psi}) is changed with the etching current density for both resistivities, but in general its values at high resistivity are higher than for the lower one; this is due to the thickness of the resulting porous layer in the silicon wafer with high resistivity which is lower than that of the low resistivity. The variation in ϵ_{psi} with the etching current density is related to the silicon dissolution in the porous layer with increasing etching current density. The width of the depletion layer (W) in the porous layer is related to N_D , ϵ and the built-in potential (V_{bi}) using equation (3). Therefore, any change in the N_d will change the depletion layer width and this makes the width of the depletion

layer inside the porous layer for the high resistive substrate is higher than the low resistive substrate. As the etching current increases the pore size increases as well as the depletion layer width. According to the C-V measurements, we can assume that the resulting junction is one-sided junction and extends in the silicon substrate side due to the depletion process in the porous layer. For the case of the wafer (2.179) $\Omega\cdot\text{cm}$, the carrier concentration changes from 1.97×10^{21} to 1.75×10^{21} ; this is related to depletion process during etching. This process occurs either because of the energy gap widening from quantum confinement, which reduces the thermal generation of free carrier or because of trapping of free carrier. A typical energy band profile of two isolated pieces of n- and p-type semiconductors and an equilibrium energy band profile of an abrupt p-n heterojunction formed by bringing them into intimate contact will be given. The porous layer exhibits n-type conductivity when it is prepared from p-type Si substrate, which has been experimentally measured using four point probe device.

It is clear that the electron affinity of wide band gap material (pS) (χ_n) is higher than that of the substrate one (c-S) (χ_p). The formation of a heterojunction with a such forbidden gap of the two materials completely overlaps then this case is called staggered. In n-PS / p-Si an isotype heterojunction, conduction is carried out almost entirely by electrons (the barrier to the transport of holes is much higher than the barrier seen by electrons) and the current will be

given by the current equation of the emission model eq (2). Figure (3 a, b, c, d) gives J-V characteristic at different cooling temperatures at the range (273-261) K^o and at the four different prepared samples of different current densities and resistivities. Figure (3a, b, c, d) gives the (saturation current density) J_0 vs $1000/T$ for different samples prepared at different current densities and different resistivities. The decrease in J leads to decrease in J_0 . The slope of this plot can give the value of the conduction band of set ΔE_c through equation (5).

Neglecting interface parameters determine, the construction of the energy band diagram for (PS/c-Si) heterojunction can be estimated by determining ΔE_v from Figure (3) with aid of equation (6) depending on the value of ΔE_c which has been found to be (0.06)eV hence the value of ΔE_v was found to be about 1.09eV. This approximation has been used by many workers see e.g. refs [4,8]. The energy of Fermi level, Fermi level position ($E_c - E_f$) and ($E_f - E_v$) are calculated using equation (4)[9,10].

Conclusion

The band line up of an isotype heterojunction with the aid of I-V and C-V characteristic at 300 K has been calculated. The band diagram shows that the formed junction behave like a simple Schottky barrier diode and the energy gap overlap formed a staggered type.

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Table (1).The obtained results from the capacitance – voltage measurements.

| Resistivity Ohm.cm | Etching currnt mA | ϵ_{ps} | Nd cm^{-3} | V_{bi} | W Mm |
|-----------------------|-------------------------|-----------------|------------------|----------|---------|
| 2.179 | 60 | 4.938 | $1.97 * 10^{21}$ | 0.33 | 2.6 |
| 2.179 | 40 | 2.457 | $1.75*10^{21}$ | 0.34 | 2.46 |
| 0.00375 | 60 | 0.776 | $1.21*10^{23}$ | 0.38 | 1.16 |
| 0.00375 | 40 | 0.956 | $1.24*10^{23}$ | 0.37 | 1.14 |

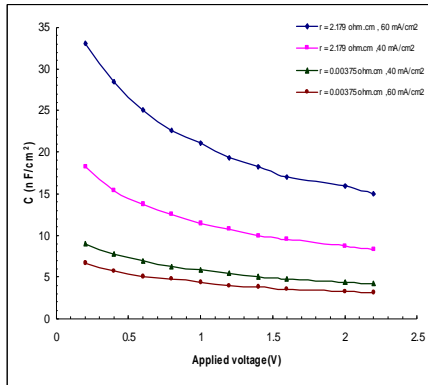


Figure (1) Junction capacitance as a function of the applied voltage.

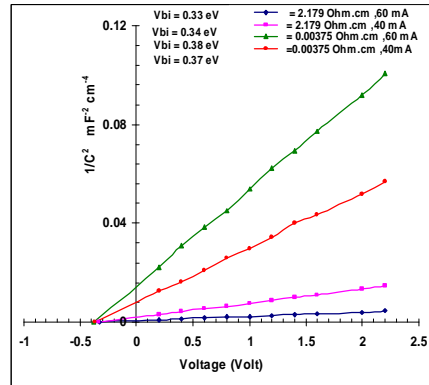


Figure (2) $1/C^2$ Vs. reverse voltage

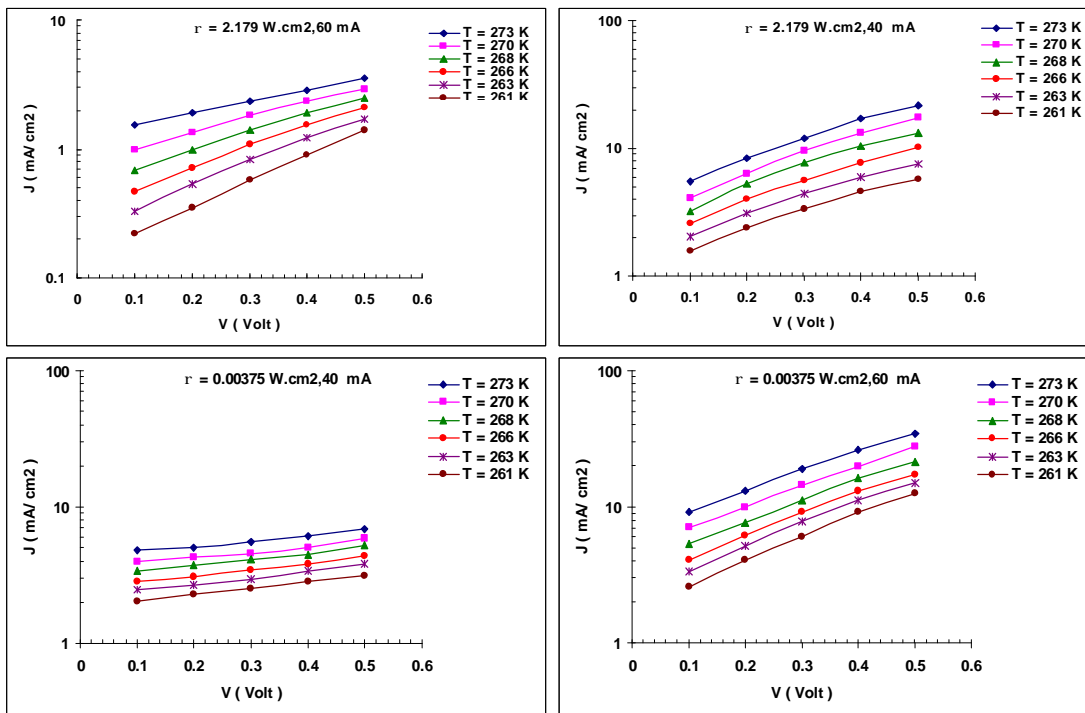


Figure (3) Current density at different cooling temperatures and at different substrate resistivities.

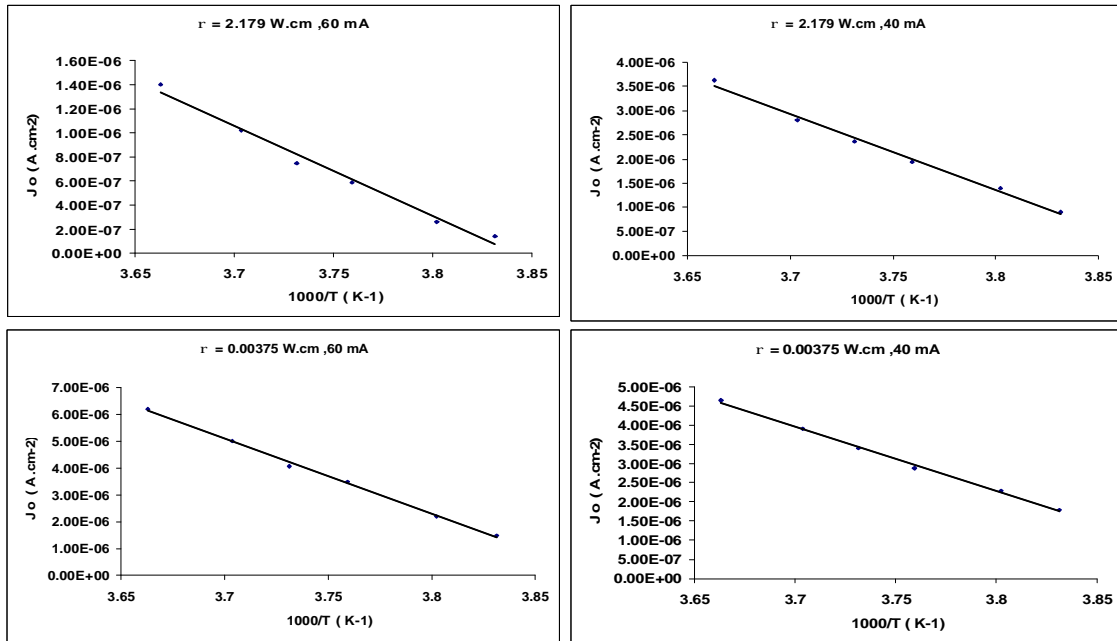


Figure (4) Saturated current density vs 1000/T and at different substrate resistivity.

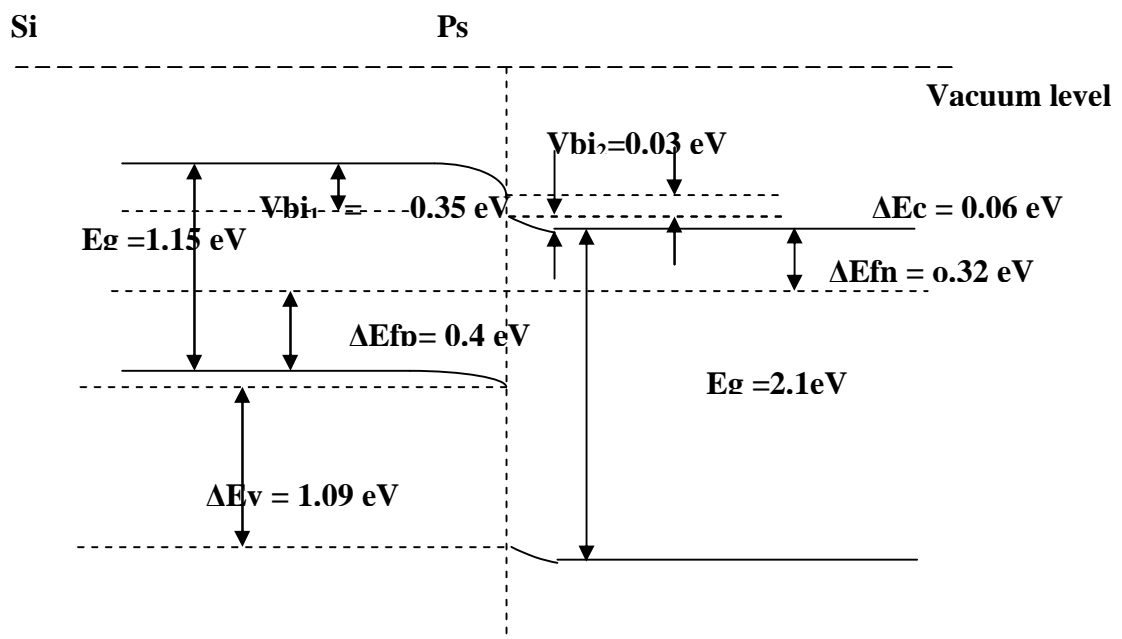


Figure (5) Energy band diagram for PSi – c-Si heterojunction device prepared at optimum condition of 60mA current density and 0.00373 Ω .cm substrate resistivity.