Carrier Life Time, Time Constant, And Other Related Detector Parameter For Porous Silicon /Silicon Heterojunction Detector

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Abstract

In the present work, Porous silicon constituting silicon nanostructures layer have been produce on crystal silicon using different preparation condition in laser induced electrical etching process. Were a (800 nm) , (1watt) semiconductor laser has been used with the electrochemical etching process to prepare the porous layer on the surface of (111) n- type silicon substrate. Two different Silicon resistivities of (0.564,4.29) Ω.cm was employed to prepared (Ps/ Si) heterojunction at different preparation condition. The characteristic of the prepared device has been found to depend directly on the formation current density and substrate resistivity. The obtained device has good parameter to work as a detector in the (V- NIR) region .

Keywords: porous silicon, heterojunction, carrier life time, detector parameter.

تحديد فترة حياة الحاملات الاقليه ، الثابت الزمني ومعلمات الكاشف الاخرى لكاشف المفرق الهجيني نوع السليكون المسامي\ سليكون

الخلاصة

في هذا البحث، تم تحظير السليكون المسامي مشتملا على السليكون ذو التركيب النانوي علىقاعده متمثله ببلوره سليكون عند شروط تحظير مختلفة. حيث تم استخدام جهاز ليزر شبة الموصل ذي الطول الموجي (800nm) وبقدره لاتتجاوز (1 watt) مع جهاز التنميش الكهروكيميائي للحصول على طبقه السليكون المسامي ، وبالتالي تحظير المفرق الهجيني نوع (Ps/Si) . تم قياس زمن النهوض للنبيطه المصنعه ووجد ليكون معتمدا على مقدار تيار التكوين. كما وجد بان النبيطه المصنعه ذات معلمات جيده للعمل ككاشف ضوئي عند المكطقة الرئيه وتحت الحمراء القريبه.

Introduction

Porous silicon (PS) is a fine network of very small voids (often called pores) surrounded by thin walls (often called nanocrystallites). PS is often synthesized from bulk (c-Si), the synthesis is started from surface of the c-Si into the bulk [3], therefore the, surface of the PS is looked to be a brittle spongy structure. The cross-section is seemed to be as a spongy skeleton, that is why the name Porous Silicon is used [4]. Heterojunction devices have been drawn a great attention in recent years mainly due to their use in optoelectronic field [5]. The heterojunction detector is one of the most important junction because of

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the wide available technique that can be used to fabricated it , beside the wide rang of radiation could be detected by using these devise [6,7,8]. Current Transport Mechanism of such Heterojunction could be explain according to the diffusion model, emission model, and the recombination model [9, 10, 11], where the relation between J and V is represented by:

$$J \propto \exp\left(\frac{qV}{hkT}\right) \qquad \ldots\ldots (1)$$

where q/kT is the reciprocal of volt equivalent of temperature and η is the diode factor. The idea of it detected ability depended on the developing of internal voltage within the depletion layer which used to separate the electron –hole pair resulting from the absorption of the light energy incident on the device surface [12]. This mechanism take a specific time depended on the device characteristic and on the preparation condition, this beside other parameters greatly affected the response time of the detector [13,14]. This is one of the most important parameter as it can limit the number of application that a given detector can use in. Several conventional quantities are often used to describe the characteristics of a given detector, these quantities include: Responsivity, Spectral response, Detectivity and D*, Quantum efficiency Linearity and Response time, which is define as the time required for the detector voltage to increase from 10% to 90% from it final value and can be given by the following equation [13,14]

$$tr = \left[tc^2 + (RdC)^2\right]^{1\backslash 2} \qquad \ldots..(2)$$

where $R_d = R_s + R_L$ & $C = C_s + C_d$

Where tc= charge collection time, Rs= series resistance, R1=load resistance, Cs= capacitance result because of electrical contact. The time constant is greatly effected by carrier diffusion time , carrier drifts time from depletion region and depletion region capacitance. The aim of this work is to measuring the rise time of Ps/Si heterojunction device at different preparation condition and then estimate the detector response time if the device which could be use as a visible –near IR photo detector and then measuring the most importing detector parameters for the optimum one.

Experiments

A commercially available P-Si of square-shaped samples each of 1x1cm2 area, of two different resistivity of (4.29, 0.564) ohm.cm were prepared using a wire-cut machine. Those samples were etched with CP4 solution consisting of (HNO3, CH3COOH, HF) (Fluke Company) of ratios (3:3:5) to remove oxides. Then they were cleaned with alcohol and ultrasonic waves produced by Cerry PUL 125 device for 15 minutes then cleaned with water and ultrasonic waves for 15 minutes. Ohmic contacts were fabricated by evaporating 99.999 purity aluminum wires using Edwards coating system. The resistivity and type of conductivity of the Si substrates were measured by using (FPP) technique. Ps samples have been produced by the laser induced electrochemical etching process were a semiconductor laser (800 nm)

wavelength and (1watt) power has been used. The samples has been prepared at different current density and two silicon substrate resistivity.

Measurements: These measure- ments include :

The rise time and time constant of the detector is measured by using (LED) with wavelength (820nm) and , the output signal is obtained using a storage scope type (8300-DCS) (programmable digital Scope) with speed (100 MHz) from (Kenwood company) The response time give by the following relation[16]:

$$t_s = \frac{t_r}{2.2} \quad \ldots\ldots\ldots (3)$$

tr= rise time

Carrier life time When the semiconductor is illuminated with photons of sufficient energy, due to the generated additional carriers, the conductivity of the semiconductor increases (resistivity will decrease).The Photoconductive property of semiconductors Can be used to determine the excessminority carriers lifetime. The experimental setup is schematically illustrated in the following figure (1).

The semiconductor sample is chosen to be a bar- shaped with a length of L And a cross-section of A. RS is the sample resistance, RL is a load resistance, VA is a dc voltage,τ is excess minority carriers lifetime, and VL is the load or Output voltage. RS, and therefore I and VL are time dependent parameters.

The measurements also include the electrical characteristics and the detector parameters such spectral responsivity were performed using a double-beam UIR-210A spectrophotometer operating within the range (0.15-1.1)μm wavelengths while the current measurements were performed using a 8010 DMM Fluke digital Multi meter. The detector para- meter include Resposivity, Specific Detectivity (D*) and Quantum Efficiency (η) also has measured and calculated.

Results and discussion

The effect of the formation current density on the value of the rise time at different resistivity cloud be shown in Figure (2). The results reveals that the formation current density plays a significant role in controlling the rise time of the device due to the effect of the porous morphology which is considered as a very important feature for many applications.

Small current density changes the flat surface of c-Si to relatively rough surface but the porous layer has a small thickness and inhomogeneous structure that reflect on the value of the rise time which found to increase. Increasing the current density to about 60 mA/cm2 produces more uniform porous layer and small wall width between pore could be observed in this case, while small feature at the top of the porous layer is formed at 20mA/cm2. Further increasing of the formation current density makes the etching rate faster and the removal of some appeared reveals the formation of a new porous layer produced by higher current density of 80 mA/cm2 and further increasing of the current density is not preferable for the porous structure production. Optimum case for the rise time of the produced porous layer is achieved at 60 mA/cm2 for low rsistivity case and at 40 mA at higher one. The photos shown in figure (3- a, b)

describe the recorded pulses from different samples prepared at (40,60) mA etching current density and at substrate resistivity of (4.2,0.56)Ω/cm respectively, were the rise time limited by the two vertical line which represent the time taken by the device Signal to rise from 10% to 90% from its final value.

Figure (3) obtained Rise time pulse for Ps/cSi heterojunction for (A-4.29 Ω.cm ,B-0.564) Ω.cm (a-20, b-40, c-60, d-80 and e-100) Ma. The high silicon resistivity appears to have larger values at smaller etching current which is related to the suitable size of the Si nanocrystillite achieved at this current besides the production of large number of contributing nanocrystals which enhance the junction properties and that is reflected in the value of the obtaind current. In the case of low eletrical resistivity the enhancement in the rise time with the increasing in the etching current density up to optimum value is clearly shown, due to the enhancement in the morphology and the porosity of the etched Si surface. At the same time, we can recognise that the rise time for the case of low resistivity is better than that of the higher one since the increasing of wafer resistivity leads to increase the etching process in the radial direction and decrease the etching toward the depth of the substrate. Therefore, the number of the Si nanocrystallites will reduce due to the excessive etching, also this attributed to the lower porous thickness layer in the case of low resistive Si. Figure (4) show the value of the estimated response time of the device that dirctly related to the value of the rise time for both samplesas a function of the etching current density.

The minority carrier life time of the prepared device as a function of formation current density could be shown in figure (5), it value give An indication about the carrier movement and diffusion length, since It related to the diffusion constant and the generation – recombination Process and the defect concentration , beside that it determined the efficiency of different device type. From this figure we can recognize that the carrier life time has a largest value at (60,40mA) for (4.29,0.564Ω.cm) substrate resistivity respectively. This is as explain above due to the enhancement in the morphology and the porosity of the etched Si surface which reflected in the improvement of the prepared devise and hence enhancement in the pours layer morphology which reduce the recombination center. From same figure we found that there is an enhancement in the value of the carrier life time toward low substrate resistivity as explain above.

Figure (6) show the obtained open circuit voltage decay pulse for devices prepared at optimum etching current density, the obtained pulse Could be devised into two special region ,the first one is the intermediate injection region at which the minority carrier concentration in the substrate Is larger than that at thermal equilibrium at the same time less than majority Carriers concentration at thermal equilibrium , as a result a Quasi- Fermi Level which directly

related to the open circuit volt as in the following equation [17]

$$qV_{oc} = \overline{F}_{fo} - \overline{F}_{fp} = k_B T \ln\left(\frac{n_p p_n}{n_i^2}\right)$$

As a result of this the recombination process take place to replace the crystal to the thermal equilibrium position. The second region present the low injection case at which the minority carrier concentration is less than it concentration at equilibrium, in this case the Fermi level close to zero, the Mass action low could be applied correctly ,i.e,

$$n \times p = n_i^2$$

For a- 4.29, b-0.56Ω.cm at 40,60mArespectivly

The current- voltage (I-V) measurements in the dark for the device prepared at optimum etching current of two different substrate resistivity are shown In Figure (7a,b)for reverse and forward biases respectively. These characteristics are very important to describe the heterojunction performance and all heterojunction parameters depending on these characteristics. In the This curves, It is clear that, high silicon resistivity appears to have larger values at smaller etching current which is related to the suitable size of the Si nanocrystillite achieved at this current besides the production of Large number of contributing nanocrystals which enhance the junction properties The spectral responsivity represents the ratio between the output generated current to the incident power and it is very important because it specifies the performance range of detector.

And that is reflected in the value of the obtained current. The rectifying behavior of the I-V characteristics of these structures may be attributed To the heterojunction potential barrier at the PS/c-Si interface. The formation of heterojunction structure in this case is due to the quantum Confinement in silicon nanocrystallites, where the porous layer has a much Wider energy gap than the c-Si and hence the PS/c-Si may be considered As a heterojunction between two semiconductors with different forbidden gaps.

Under reverse bias, for all cases, it is clear that the curve contains two regions; the first is the generation region where the reverse current is slightly increased with the applied voltage and this leads to generate electron- hole pairs at low bias. In the second region, a significant increase can be recognized when the reverse bias is increased. In this case, the current results from the diffusion of minority carriers through the junction. We can also note from this figure the rapid incremental in the reverse Current at high reverse voltage, which is probably due to the leakage Current arising from the surface layer. The enhancement in the reverse Current at low resistivity is related to enhancement in the junction structure, Which results in reducing the number of defects at pS/c-Si interfaces of the junction. These defects result from the strain due to crystal structure. In the forward bias, the Forward voltage results in reducing the height of the potential barrier, therefore, majority carriers are able to cross the potential barrier much easier

Than at zero bias, so that the diffusion current becomes greater

than the drift current. Short-Circuit Current and Open- circuit Voltage as a function of the incident photon power of the halogen lamp for both samples of different substrate resistivities and different etching current densities are given in Figures (8a,b). We can recognize that the value of the open circuit voltage and also the short Circuit current at lower substrate resistivities higher than that at high substrate resistivity and this normally results since the open circuit voltage is Linearly proportional to the generated photocurrent as given in the following equation, and also, depends on the thickness and the porosity of the silicon nanocrystallites layer [16].

$$V_{oc} = \frac{K_B T}{q} \ln\left[\left(\frac{J_{se}}{J_o}\right) + 1\right]$$

We can also recognize the linear relation between ISC and VOC to a maximum value beyond which both values tend to saturate and become constant, this made it useful to use as a detector. This occurs due to the total separation Of the photo-generated electron- hole pairs at the depletion region at the interface between the PS and c-Si. The difference in the value of Voc and Isc at different etching current density is related to the Is nanocrystallites Layer thickness and the porosity which itself is greatly affected by the etching current density. The results also show that the short current and open circuit

Voltage saturate at high power density since the electric field is strong enough to separate any generated pair for a given incident power. Figure (9) gives the responsivity as a function of wavelength for sample prepared at optimum conditions that have minimum respone time and hence the larger resonce speed.

In this junction, we can recognize three different regions on the curve. The first one (short wavelengths) implise a considerable increase in the responsivity and this increase relates to the high absorption coefficient. This leads to lower absorption depth and fast recombination process compared with any other region inside the material and this is called the probability of carrier concentration, which increases with the departure from the surface region, which means rise the responsivity in this region followed by decrease in responsivity value which is related to the large surface recombination processes. In the second region(700-900nm), we observe the highest value of the wavelength-dependent responsivity as these wavelengths are absorbed at the active region of the junction interface (depletion region) and along a distance equal to the diffusion length of minority carriers. At this region, the generated electron-hole piars move due to the internal electric field beside the negligible recombination process in this region. The maximum responsivity appears at 800 ± 50nm despite the fact that this region is far from the cutoff wavelength. This happens in order to coincide with mass action law[15]. In the third region, (>850nm), the incident light is absorbed within the material where the bulk recombination processes take place, so the carrier concentration probability can exist in

this case leading to lower responsivity. Because the PS semiconductor has a wide and direct band gap, it could be used to collect high energy photons. This makes the heterostructure of PSi/Si suitable for use as (V-NIR) detector. Also, the photons of lower energy than UV will be collected at the semiconducting material of the base after being transmitted through PS surface layer. Figure (10) shows the quantum effeciency of the detector as a function of wavelength. The increase in the photocurrent is attributed to the same reasons of the responsivity. In Ps/Si device, the interfacial layer is taken to be a wide-band gap which acts as a tunneling barrier for carrier transport from one side of the junction to the other. The figure of merit of the detectors D* is defined as the root mean square (r.m.s.) of the signal to noise ratio (SNR) in 1Hz bandwidth per unit r.m.s. incident radiant power per sequre root of the detector area. The specific detectivity versus wavelength is for heterojunction devices,dirctly related to the value of resposivity So, we can recognize a similarity in the obtained behavior. The most important parameter that specifies the detectivity for a given detector is the noise current (In) that is found to be about (1.2 *10-14)A for high resistivity and (0.5*10-14)A for low resistivity. All detectors are limited to the minimum radiant power that can be detected in the form of noise, which may arise at the detector itself, in the radiant energy to which the detector responds, or in the electronic circuit following the detector.The most common built-in noise whithin the detector are white noise, Johnson noise and thermal niose, which arises from the random motion of the current carriers within any resistance material. Also, other most important source of noise is the generation-recombination noise that results from the presence of defects acting as trapping centers. As a result the D* take it values depending on the values of In and responsivity as shown in figure(11).

Conclusions

Formation current density plays a significant role in controlling the device rise time due to it effect on porous morphology; Optimum case for the rise time at formatin current density of (60 mA/cm2 , 40 mA/cm2) for (4.29,0.564 Ω.cm) resistivity respectively. This result directly affected the estimated value of the device response time and related detector parameter.

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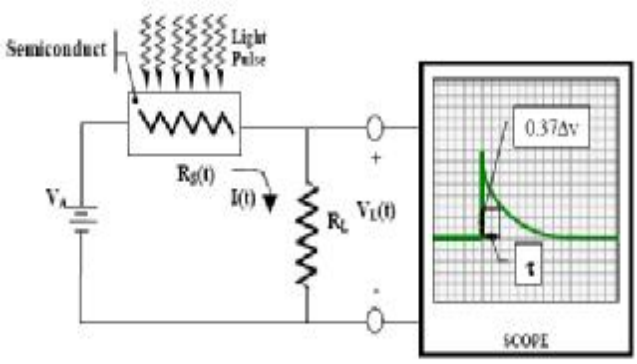

Figure (1) carrier life time measurement experimental set upset up

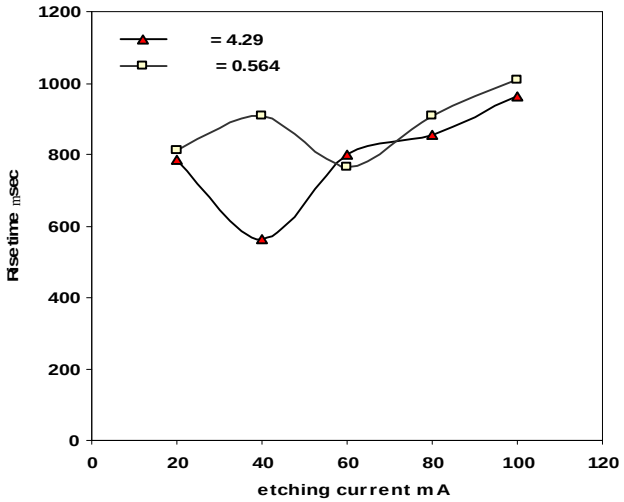

Figure (2) device rise time as a function of formation etching current at different resistivity

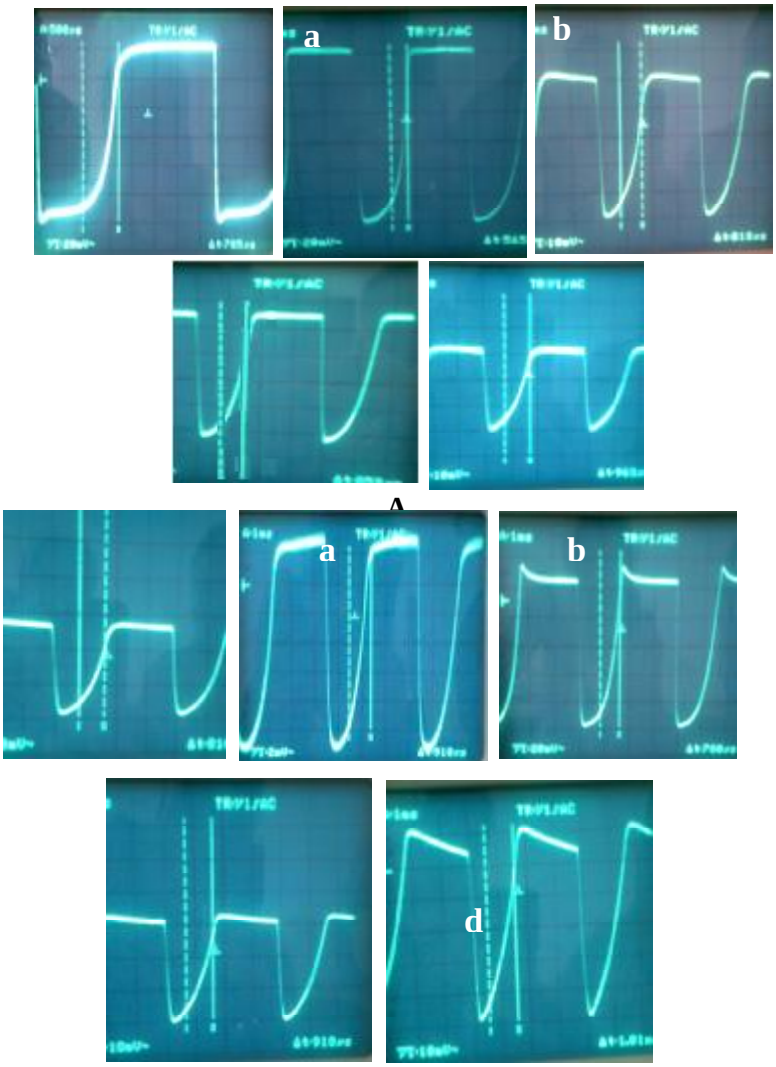

Figure (3) obtained Rise time pulse for Ps/cSi heterojunction for (A-4.29 W.cm ,B-0.564) W.cm (a-20, b-40, c-60, d-80 and e-100) mA

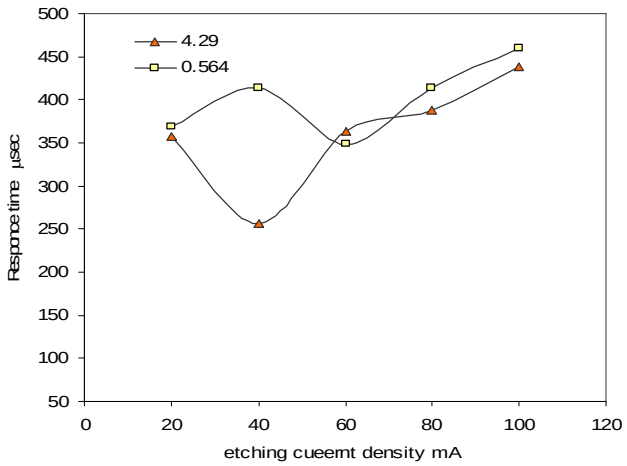

Figure (4) device rise time as a function of formation current density

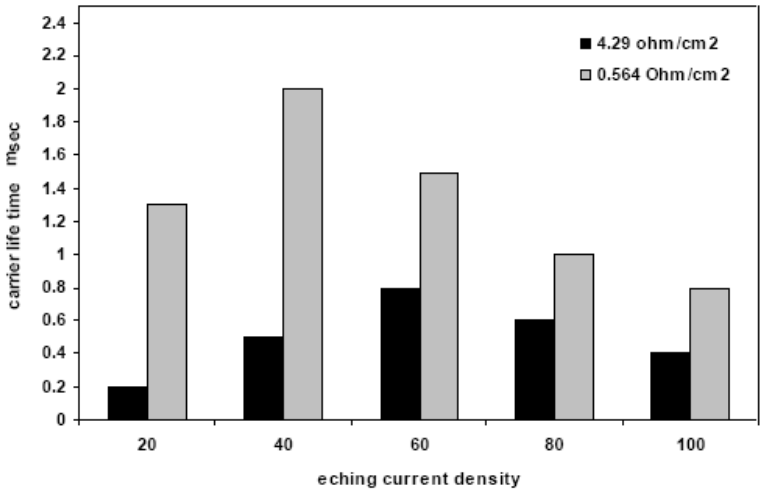

Figure (5)Minority carrier life time as a function of etching current density

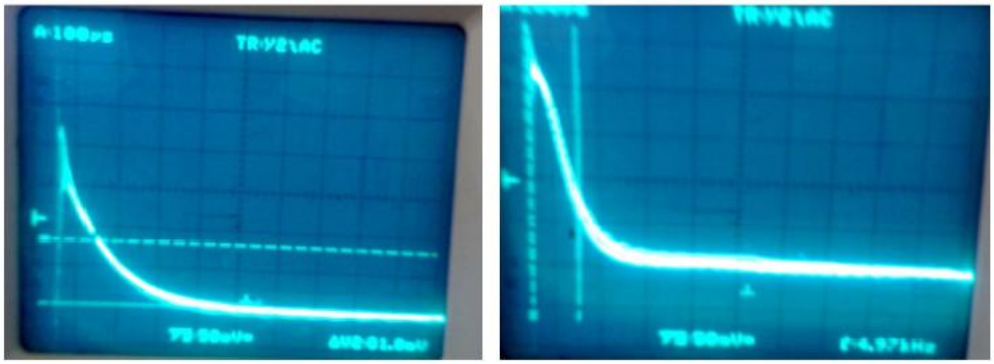

Figure (6,a,b) Obtained open circuit voltage decay pulse for Ps/cSi heterojunction
For a- 4.29, b-0.56Ω.cm at 40,60mArespectivly

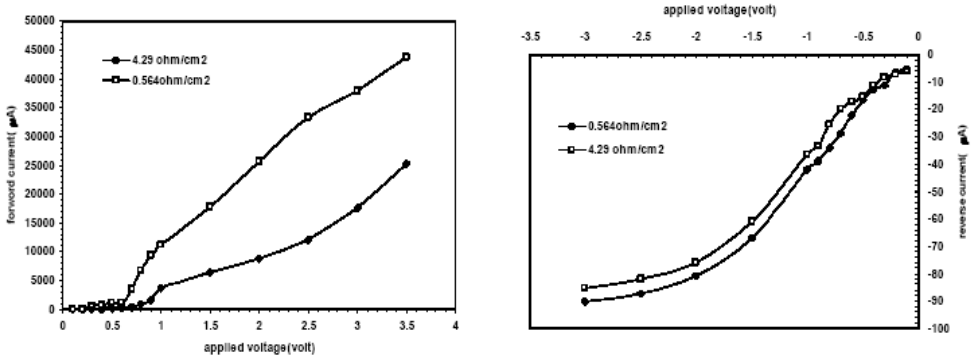

Figure (7a,b)current _voltage characteristics at forward and reverse biases For Ps/cSi heterojunction for a-4.29,b-0.56Ω.cm cm at 40, 60 mA respectively.

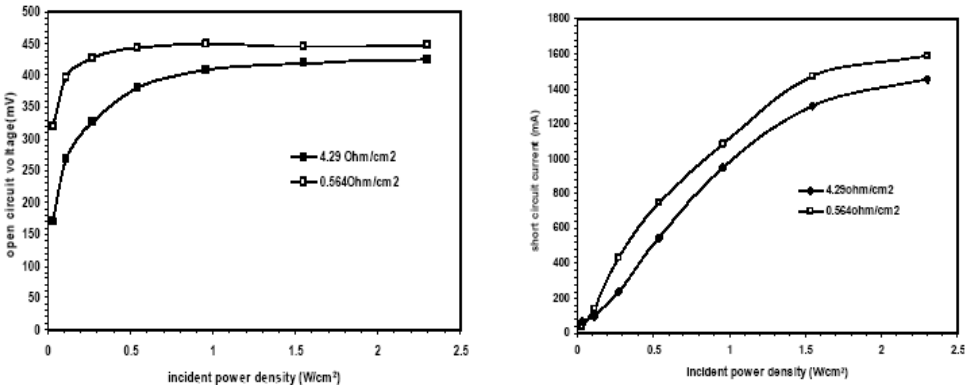

Figure (8a,b)Open circuit voltage and short circuit current as a function of the incident photo energy for different substrate resistivities and different etching Current densities.

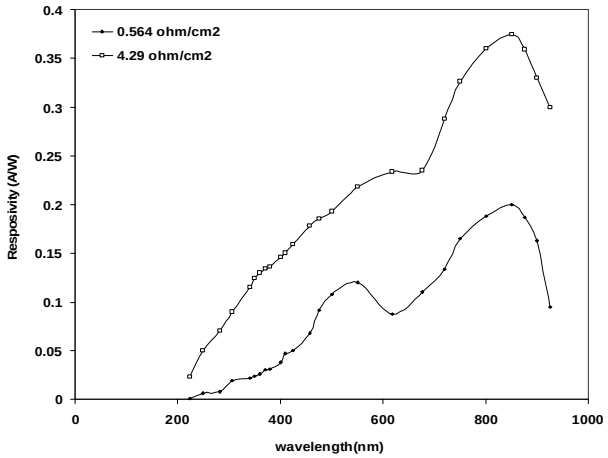

Figure (9) The spectral responsivity as a function of the incident wavelength at optimum current density of (60,40mA) for(0.564W/cm^2,4.29W/cm^2) substrate resistivity repectivly formed Ps/Si heterojunction

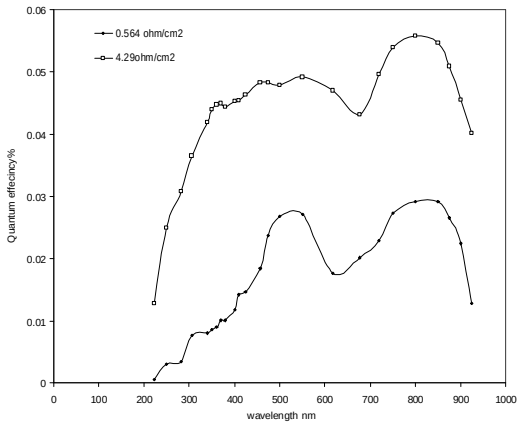

Figure (10) The Quntum effecicncy as a function of the incident wavelength at optimum current density of (60,40mA) for($0.564W/cm^2$,$4.29W/cm^2$) substrate resistivity repectivly