Design and Simulation of Digital PLL Synchronizer for BPSK and QPSK Based on Software Defined Radio

Dr. H. T. Ziboon* & **A. A. Thabit****

Received on:16/10/2008
Accepted on:2/4/2009

Abstract

This paper presents a design and simulation of digital PLL synchronizer, using Costas loop based on SDR for high frequency communication systems. Design parameters are selected for each unit of the proposed systems in order to accommodate SDR requirements. Different techniques for carrier recovery based on SDR are discussed. PLL techniques is chosen for synchronization, since it is one of the most active synchronization techniques. BPSK and QPSK synchronizers for coherent receivers have been designed and simulated based on SDR using both Costas loop and modified Costas loop. The simulation result shows that these two systems are reliable in recovering the carrier phase and frequency when significant frequency and phase are present. Simulation result shows that the BPSK system has $P_e = 10^{-3}$ at E_b / N_o equal to 8.5 dB in the presence of AWGN and has the ability to track frequency offset up to 1200Hz with $2*10^{-4}$ probability of bit error at E_b / N_o equal to 20 dB. This system can track phase offset 45^o with $P_e = 10^{-4}$ at E_b / N_o equal to 20 dB. For QPSK system, the probability of bit error 10^{-3} at $E_b / N_o = 9\,dB$ and has the ability to track frequency offset 300 Hz and phase offset=9^o with $P_e = 10^{-3}$ at E_b / N_o equal to 20dB.

Keywords: SDR, PLL, Synchronization, Carrier recovery, Costas loop.

تصميم و محاكاة حلقة قفل طور رقمي مزامن للمفاتيح المتغيرة الطور الثنائية والرباعية بالاعتمادعلى برمجيات التعريف الراديوية

الـــخـــلاصـــة

يتضمن هذا البحث تصميم ومحاكاة حلقة قفل طور بالاعتماد على منظومة راديوية تعمـــل بالبرامجيات لاغراض التزامنية لأنظمة الاتصال العالية التردد. متغيرات التصميم تم اختيارهـــا لكل وحدة في المنظومة المقترحة لغرض استيعاب متطلبات المنظومة الراديوية البرمجيـــة. تـــم مناقشة عدة تقنيات لاستعادة تردد وطورالحامل. تم اختيار تقنية حلقة قفـــل الطـــور لاغـــراض التزامنية لأنه أحد ابرز تقنيات التزامنية. تم تصميم ومحاكاة المفـــاتيح المتغيـــرة الطـــور الثنائيـــة والرباعية بالاعتمادعلى SDR بواسطة حلقـــة كوســـتاس (Costas loop). اوضـــحت نتـــائج المحاكاة اداءً موثوقا باستعادة طور وتردد الحامل عند وجود تغيير بالتردد وبالطور حيث يمتلك نظام المفاتيح المتغيرة الطور الثنائية احتمالية خطأ بالبت $P_e = 10^{-3}$ عند E_b / N_o مقـــدارها 8.5dB بوجود AWGN. للنظام القدرة على مجاراة تـــردد تغييـــر الـــى 1200Hz بأحتماليـــة خطـــأ

* Electrical and Electronic Engineering Department, University of Technology / Baghdad
**Computering Communication Engineering Department, AL Rafidain University College / Baghdad

https://doi.org/10.30684/etj.27.10.9
2412-0758/University of Technology-Iraq, Baghdad, Iraq

بالبت 10^{-4}*2عند E_b / N_oمقدارها 20dB وله القدرة على مجاراة تغيير بالطور مقداره 45 درجة باحتماليةخطأ بالبت $10^{-4} = P_e$ عند E_b / N_oمقدارها 20dB اما بالنسبة لنظام المفـاتيح المتغيـرة الطور الرباعية فأن النظام يمتلك احتمالية خطأ بالبت مقدارها 10^{-3}عنـد E_b / N_oمقـدارها 9dB وله القدرة على مجاراة تردد 300Hz باحتمالية خطأ بالبت 10^{-3} وطور تغيير مقداره 9 درجـة باحتمالية خطا بالبت 10^{-3}عند E_b / N_oمقدارها 20dB.

1. Introduction

Wireless communications is the fastest growing segment of the communications industry. The vision of wireless communications supporting information exchanged between people or devices is the communications frontier of the next century. This vision will allow people to operate a virtual office anywhere in the world using a small handheld device with wireless devices [1]. Traditional wireless devices are designed to deliver single communication service using a particular standard [2]. It is expensive to upgrade and maintain a wireless system each time a new standard comes into existence. Wireless systems are gravitating towards minimal radio hardware designs using flexible architecture software radio (SR) [3]. Software defined radio (SDR) is a collection of hardware and software technologies that enable reconfigurable system architectures for wireless networks and user terminals to reduce the amount of analogue signal processing in radio applications, by implementing the conversion between analogue and digital signals as close to the antenna as possible, and then performing signal processing operations in the software domain [2]. SDR can be viewed as an adaptive solution for making wireless networks highly flexible [4]. The concept of SDR has initially been discussed for military applications. Today, with the increase of the digital signal processor (DSP) capabilities on the one hand and the requirements for rapid deployment to market on the other, SDR is emerging as an important commercial technology. It brings together two key technologies of the last decade: digital radio and downloadable software [5]. Over time the number of system components performed in software is increasing. Figure (1) depicts the evolution from Hardware (HW) to SDR to SR to "Adaptive Intelligent-Software Radio" (AI-SR) [3].

Synchronization is one of the most difficult problems for the communication systems. The phase and frequency offsets are the critical problems for the data detection that lead to severe performance degradation especially when higher order modulation is applied. These two offsets can be compensated by using phase locked loop (PLL) which represents the heart of nearly all synchronization systems. PLL has a relatively simple structure composed of phase detector, loop filter and voltage Controlled Oscillator (VCO) [6]. An important technique is the combination of two quadrature loops to form Costas loop which are discussed in the next sections.

2. Phase locked loop (PLL)

2.1 Analog PLL

The heart of nearly all synchronization systems is some version of phase locked loop (PLL) [6]. Analog PLL consists of three components [7,8]: the phase detector

(PD), the loop filter (LF) and the voltage controlled oscillator (VCO).The function of PD block is to compare the phases of the input and output signals and generate an error signal proportional to the phase deviation between them. There are two forms of phase detector which are the analog PD and digital PD. Basically analog PD functions as a mixer with an IF centered at zero frequency [9], while digital PD are based on applications of simple flip-flop gates or more complicated combinations. Low-pass filter is used to remove the high frequency terms that comes from the output of the PD [10]. The selection of the loop filter is a very important decision, since it will determine the behavior and characteristics of the PLL under various operating conditions such as bandwidth, lock-in range, pull-in range, pull-out range and hold-in range of the PLL during operation [11]**.** Active low pass PI filter was selected due to its great performance and its stability [8]. The final component is the VCO which is a device that produces the carrier replica i.e. a sinusoidal oscillator whose frequency is controlled by the input voltage [6]. The control voltage from the loop filter adjusts the frequency and phase of the VCO to synchronize with the input signal's frequency and phase. In the locked state the frequency difference and the phase difference between the input signal and the output signal from the VCO is zero. This means that the PLL replicates a signal whose frequency and phase are exactly the same as those of the input signal [10].

2.2 Digital phase locked loop (DPLL)

DPLL are attracting more attention for the significant advantages of digital systems than analog PLL. These advantages include superiority in performance, speed, reliability, and reduction in size and cost. DPLL reduced many problems associated with APLL [12]. Figure (2) shows the digital form of PLL. In DPLL the VCO is replaced with digital direct synthesizer (DDS), the loop filter is digitized and is converted to IIR filter and finally the PD converted from a simple mixer to digital PD. There are four types of digital PD: Flip-Flop DPLL, Nyquist-rate DPLL, lead-lag DPLL, exclusive-OR DPLL and zero-crossing DPLL [13, 14]. In this paper the flip-flop DPLL is used to provide the phase and frequency output error signal.

3. Carrier recovery

Synchronization is one of the fundamental functions in communication systems. Its task is to lock the synchronization parameters of the receiver with the received signal. Most receivers require three main synchronization levels: carrier synchronization, symbol synchronization and frame synchronization [6]. Estimation of synchronization parameters is very essential for performing demodulation and detection of the data from the transmitted signal with high reliability.

In almost every receiver or demodulator performance, some level of signal synchronization is generated. In the case of binary phase shift keying (BPSK) and quadrature phase shift keying (QPSK) demodulation, the receiver is assumed to be able to generate reference signals whose phases are identical to those of the signaling alphabet at the transmitter [6,15,16]. In this paper Costas loop and modified Costas loop are selected to synchronize the BPSK and QPSK

signals because they are a convenient mechanism for suppressed-carrier tracking.

4. System Description

The BPSK Costas loop block diagram [6] is depicted in figure (3). The BPSK signal is first generated at the transmitter, then after the multiplier, passed through the arm filters in order to suppress the higher order components and the low order components is passed then the two filtered signals is passed through the loop filter which is the lead-lag type. The signal that leaves the loop filter then is passed through the VCO to generate the carrier signal necessary for synchronization purposes. For QPSK signal, the modified Costas loop [8,18] is used in order to accommodate the QPSK requirements as shown in figure (4). The design parameters of the system are shown in table (1). Design parameters are either selected from the design standard requirements or according to results analysis of each system unit.

5. Description of the Designed system components

5.1 Design of Loop Filter

The analog PI filter is used as mentioned due to its stability in canceling the error that comes from the multiplication process. This filter generates the VCO control voltage according to the error from the multiplication. The transformation from S-domain to Z-domain is used in the design of the loop filter as shown below. The design parameters of the loop filter is shown in table (2).

The transfer function of the PI filter is [8]:

$$F(s)=\frac{1+st_2}{st_1} \qquad \dots (1)$$

The relation between Z and S is [8,11]:

$$s=\frac{2}{T}.\frac{1-Z^{-1}}{1+Z^{-1}} \qquad \dots (2)$$

Substituting equation (2) by (1) yields:-

$$F(z)=\frac{\frac{2t_2+T}{2t_1}+\frac{T-2t_2}{2t_1}.z^{-1}}{1-z^{-1}}=\frac{b_o+b_1z^{-1}}{1-z^{-1}} \dots (3)$$

From the 2nd order PLL relation [7,8]:

$$H(s)=\frac{2Vw_ns+w_n^{\ 2}}{s^2+2Vw_ns+w_n^{\ 2}} \qquad \dots(4)$$

Where: T is the sampling time

t is the time constant

b_o and b_1 are loop filter coefficients

$$2Vw_n=\frac{K_dK_ot_2}{t_1},\text{and}$$

$$w_n^{\ 2}=\frac{K_dK_o}{t_1}$$

V is the damping ratio

w_n is the natural frequency in rad/sec

K_d is the PD gain in volt/rad

K_o is the DDS gain Hz/volt

The results must comply with the relation $t_1=at_2$, where a is a constant such that $a > 2$ [8,11]. This relation was obtained by calculating the 3−dB frequency of the loop filter [8]:

$$W_{LF\_3db}=\frac{1}{\sqrt{0.25t_1^{\ 2}-t_2^{\ 2}}}$$ in order to make sure that $\sqrt{0.25t_1^{\ 2}-t_2^{\ 2}}>0$,

$t_1>2t_2$ Which result in a >2

$t_1>>2t_2$

Gardener [7] suggests that there is a relation between t_1,t_2.

$a=\frac{K_dK_o}{2Vw_n}$, let w_n=500 rad/sec, V =0.7

$$\therefore a = \frac{100{,}000}{2(0.7)(500)} = 142.86$$

i.e. $t_2 = \frac{2V}{w_n} = \frac{2(0.7)}{500} = 0.0028$

$\mathbf{Q}\, t_1 = a t_2 \qquad \therefore t_1 = 142.86 t_2$

$\Rightarrow t_1 = 0.4$

Substituting by equation (4) yields:

$$H(s) = \frac{700s + 250e^3}{s^2 + 700s + 250e^3} \qquad \ldots (5)$$

Using the values previously calculated for t_1, t_2 and T we find that $b_o = 7.0000417e-3$, $b_1 = -6.9999583e-3$. This can be approximated to be $b_o = 0.007$ and $b_1 = -0.007$.

5.2 Phase Detector Design

The tri-state-based flip-flop DPLL consists of two D flip-flops with additional logic to reset the latches is chosen. The PFD generate pulses to steer the VCO frequency either up or down. Any mismatch between the up and down paths of its output degrades the linearity of its phase error characteristic. The PFD output depends on the phase error and the frequency error [16,17].

5.3 Design of VCO

In the digital domain, the VCO is replaced by the digital direct synthesizer (DDS) [14]. In this paper the DDS is used in the SDR synchronizer system as shown in figure (5). The characteristics of the DDS are shown in table (3).

5.4 Design of arm filter

The arm filter is a low pass filter in order to remove the high frequency components that come from the multiplication of the received signal and the VCO signal for both I and Q channels. In this paper the FIR filter is chosen in the design because it has linear phase response [19]. The characteristic of this filter is shown in table (4). The Hamming window is selected in the design. The transfer function for this filter is given by [8]:-

$$H(z) = \sum_{n=0}^{N-1} h(n) z^{-1} \qquad \ldots (6)$$

The hamming window takes the form [8]:

$$w(n) = 0.54 + 0.46\cos\left(\frac{2pn}{N}\right) \qquad \ldots (7)$$

Where:- N is the filter order

$h(n)$ is the impulse response, n=0,1,…N-1

$h(n) = h(0), h(1), h(2) \ldots h(N-1)$

6. Simulation Results

6.1 PLL measurements

Figure (6) represents the flow chart of the designed system. Figure (7) shows the simulation results of general PLL block diagram when there is 10 deg. phase offset between the input and the DDS signals. Figure (8) represents the loop filter output for 10 deg. Offset.

6.2 BPSK system simulation results

The performance of the designed system will be evaluated by plotting the probability of bit error (P_e) versus the E_b / N_o and the output of the loop filter which indicates the error level. Theoretically the relation between E_b / N_o and P_e for BPSK are represented by the relation [20]:-

$$P_e = Q\left(\sqrt{\frac{2E_b}{N_o}}\right) \qquad \ldots (8)$$

and for QPSK is:-

$$P_e = 2Q\left(\sqrt{\frac{2E_b}{N_o}}\right) \qquad \ldots (9)$$

Q is the error function.

Figures (9,10 and 11) show the P_e versus E_b / N_o for different values of frequency offsets from 0 offsets to

1500 Hz. Figures (12 & 13) show the loop filter outputs for two cases 100Hz and 300Hz frequency offsets.
Another test to check the performance of the system is to change the phase between the input and the DDS signal while the frequency is kept constant. Figure (14) represents the cases when there are phase offsets extending from 0 deg. to 45 deg.
The final test represents the behavioral of the system when the phase and the frequency are changed together at the same time. Figure (15) represents the cases when 50Hz and variable phase offsets while figure (16) represents the cases when 100Hz and variable phase offsets. Finally figure (17) represents the cases when 200Hz and variable phases. Figure (18) shows the input and the output of the designed FIR filter.

6.3 QPSK simulation results

Figure (19) shows signal waveforms of the simulated QPSK transmitter.
Figure (20) shows the simulation results of the QPSK system with different frequency offsets from the ideal case starting from the 0 offset up to 1000Hz frequency offset. Figure (21) shows the simulation results of the QPSK system with different phase offsets from 2^o to 18^o. Figure (22) shows the cases when 50Hz frequency offset and variable phase offsets (0^o to 18^o).

6.4 Discussion of simulation results

1. The designed BPSK system has a probability of bit error equal to 10^{-5} at 11.5 dB without any frequency or phase offset.
2. The designed BPSK system is capable of tracking the phase offset up to 45 degree
with 10^{-4} probability of bit error at E_b / N_o equal to 20dB and can also track the frequency offset up 1200 Hz with $2*10^{-4}$ probability of bit error at E_b / N_o =20dB.
3. The designed BPSK system has the ability to track the phase and frequency offsets in specified ranges extending from 50 Hz and 5^o with $P_e=10^{-4}$ at E_b/N_o =15 dB up to 1000Hz and 9^o with $P_e=10^{-3}$ at E_b/N_o =19 dB which shows the loss in E_b/N_o as a penalty that may be paid to overcome the offsets.
4. The designed QPSK system has a probability of bit error=10^{-5} at 12 dB without any offset.
5. The designed QPSK system can track the phase offset up to 9 degree phase offset with a probability of bit error 10^{-3} at E_b / N_o =20dB and can track the frequency offset up to 300 Hz frequency offset with a probability of bit error =10^{-3} at E_b / N_o equal to 20dB.
6. The designed QPSK system has the ability to track the simultaneous frequency offset and phase offset in the range from 50Hz and 2^o offsets with $P_e=10^{-3}$ at E_b / N_o equal to 15.5dB up to 300Hz and 2^o offset with $P_e=2*10^{-2}$ at E_b / N_o equal to 20dB.

7. Conclusions

The conclusions of this work can be summarized as follows:-
1. The carrier recovery technique based on SDR presented in this paper proved to be applicable to the modulation schemes of M-PSK signals. Simulation has shown that frequency and phase estimation can be implemented by using feedback structures (Costas loop) with a large estimation range and good performance. In order to obtain

reasonable values of the probability of bit error degradation, it is required that the frequency error be a small fraction of the symbol rate.
2. The designed 2nd IIR loop filter works perfectly to eliminate the errors.
3. The Hamming window used in the arm filter to obtain matched filters.
4. DDS is the best choice to implement SDR systems.

8. References

[1].Andrea Goldsmith, ‘‘Wireless Communications’’, Stanford University, Andrea Goldsmith Publishers, 2004.
[2]. F. A. Sabir "Modeling of Software Defined Radio transceiver", Ph.D. thesis, Department of Electrical and Electronic Engineering, University of Technology, Iraq, 2008.
[3]. P. B. Kenington "RF and Baseband Techniques for Software Defined Radio", Artech House, INC., 2005.
[4]. A. A. Abidi, "The Path to the Software-Defined Radio Receiver", IEEE Journal of solid state Circuits, vol.42, No. 5, pp. 954-966, May 2007.
[5]. S. O. Tatu, E. Moldovan, Renato G. Bosisio, Tayeb A. Denidni " Ka-Band Analog Front-End for Software-Defined Direct Conversion Receiver", IEEE Transactions on Microwave theory and techniques, vol. 53, No. 9, pp. 2768-2776, September 2005.
[6]. B. Sklar, "Digital Communications Fundamentals and Applications", Prentice Hall, Englewood Cliffs, New Jersey, 2001.
[7]. F. M. Gardner, "phase lock techniques", 3rd edition, John Wiley, New York, 2005.
[8].R. E. Best, "Phase locked loop design, simulation and applications" McGraw-Hill publishers, 2003.
[9]. A. Posri, "Phase Locked Loop Design for Transmitting and Receiving Sections in Optical Wireless Access", M.Sc. thesis, Kochi University of Technology Kochi, Japan February, 2005.
[10]. P. Lian, "Improving Tracking Performance of PLL in High Dynamic Applications", M.Sc. thesis, Department of Geometrics Engineering, university of Calgary, Alberta, November 2004.
[11].D.P.Feliciano, "Digital implementation of second order Costas loop demodulator", M.Sc. thesis, University of Puerto Rico, 2004.
[12]. S. R. AL-Araji, Z. M. Hussain and M. A. AL-Qutayri, "Digital Phase Lock Loops Architectures and Applications", Springer publishers, 2006.
[13].R. Brady, "Across platform framework for software defined radio", M.Sc thesis, stellenbosch university, March 2007.
[14].V. Daita, "Behavioral VHDL Implementation of Coherent Digital GPS Signal Receiver" M.Sc. thesis, Department of Electrical Engineering College of Engineering University of South Florida, 2004.
[15].Y. Linn, "Synchronization, phase detection, lock detection and SNR Estimation in Coherent M-PSK Receivers", Ph.D. thesis, University of British Colombia, July 2007.
[16]. S. P. Nicoloso, "An investigation of carrier recovery techniques for PSK modulated Signals in CDMA and multipath Mobile environments", M.Sc. thesis, the Faculty of the Virginia Polytechnic Institute and State University, Bradley Department of Electrical Engineering, June 1997.
[17]. D. C. Al-Azzawi, "Implementation of digital phase locked loop for suppressed Carrier *recovery using TMS320C25*", M.Sc thesis, university of Baghdad, Iraq 1998.

[18].R. Kippenberger, "On Real Time Digital Phase Locked Loop Implementation with Application to Timing Recovery", M.Sc thesis, University of Canterbury, Christchurch, New Zealand, November 2006.
[19]. J. VANKKA "Digital synthesizers and transmitters for software radio", Springer 2005.
[20]. J. B. Anderson, "Digital transmission Engineering" 2nd Edition, Lund University, IEEE Press Series on Digital & Mobile Communication, 2005.
[21] E. Hagemann, "The Costas Loop – an Introduction" technical report, 2001.

Table (1) Design parameters goals

Parameter	Selected type or values	comment
Multiplier	PFD-type	PFD is chosen to provide error signal phase and frequency [12]
IF frequency	10 MHz	Max frequency can be used to implement the SDR system.
Arm filter	FIR type	Because it has linear phase response
Loop filter	Second order IIR filter	Can be removed if the arm filters are matched [21]
DDS	Free running frequency is 10MHz	The initial frequency when the system is locked.
Sampling frequency	100 MHZ	This value is selected for butter simulation results
Data rate	5 Mbps	Suitable data rate can be selected for IF

Table (2): Characteristics of the loop filter

Bandwidth	100 KHz
Type of filter	Digital IIR LPF
Filter order	2nd order

Table (3): Characteristics of the DDS

DDS	In order to recover the phase and frequency together [6]
DDS gain (k_o)	100 kHz/V [8]
f_o	10MHz

Table (4): Characteristics of the arm filters

LPF	To remove high frequency components from output of PFD[8]
FIR	Because it is a linear phase response, and simple in the design
Bandwidth (BW)	5MHz
Hamming window is used	Because of its simplicity and for its accuracy
Filter order	15

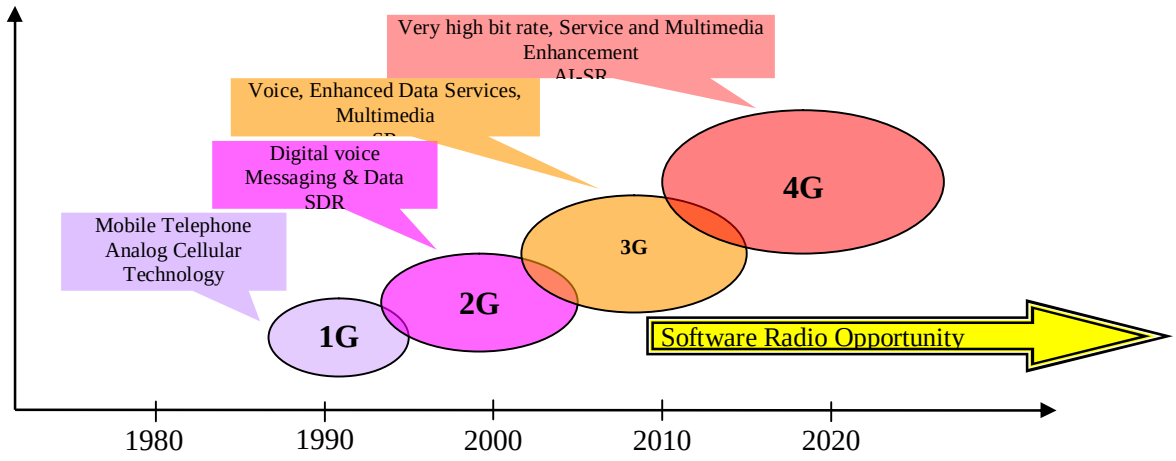

Figure (1): SDR opportunity window

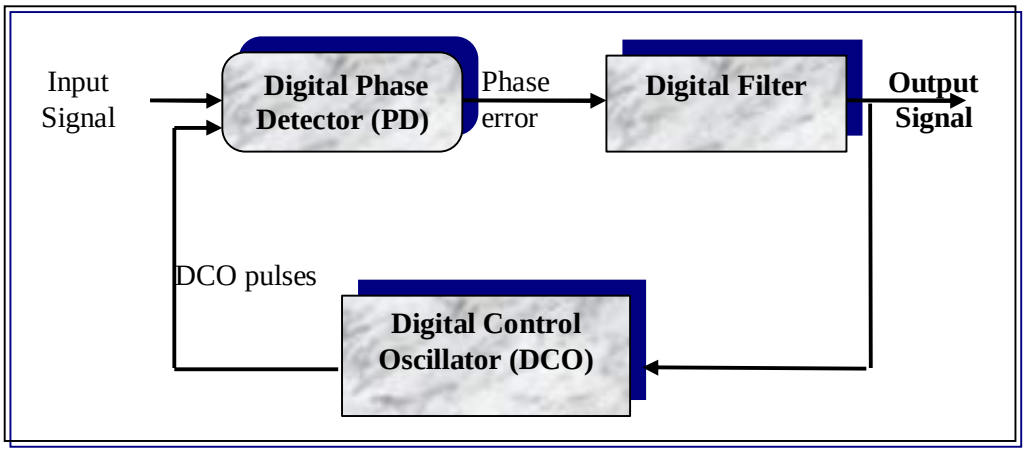

Figure (2): Block diagram of digital phase locked loop

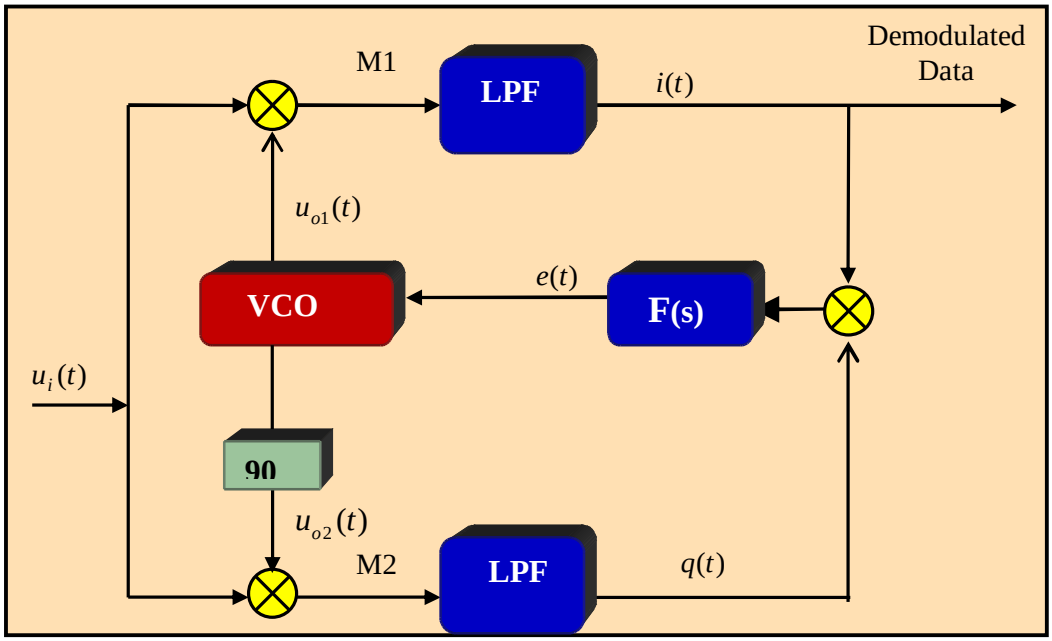

Figure (3) The conventional Costas loop for BPSK

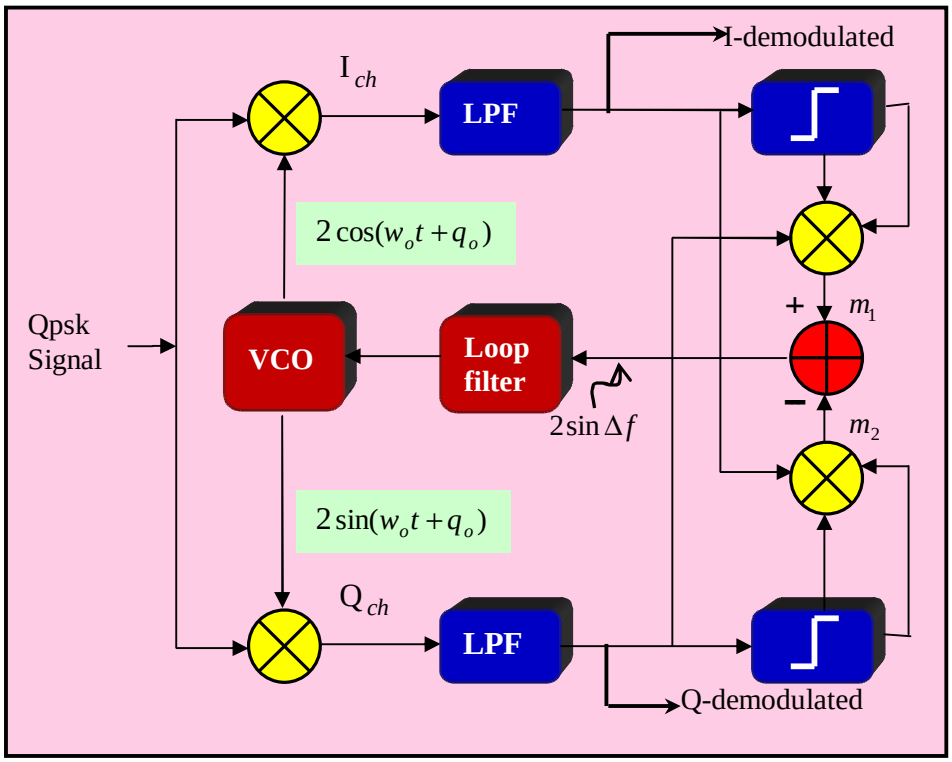

Figure (4) Costas loop for QPSK synchronizer

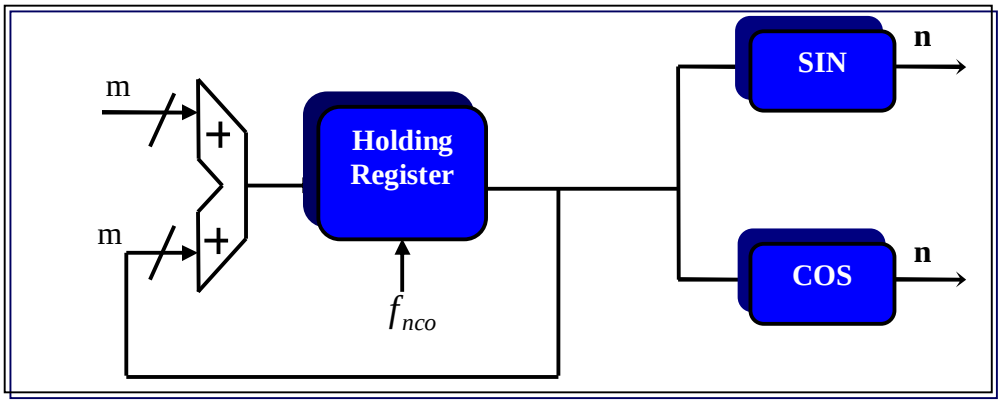

Figure (5) Direct digital frequency synthesizer (DDS)

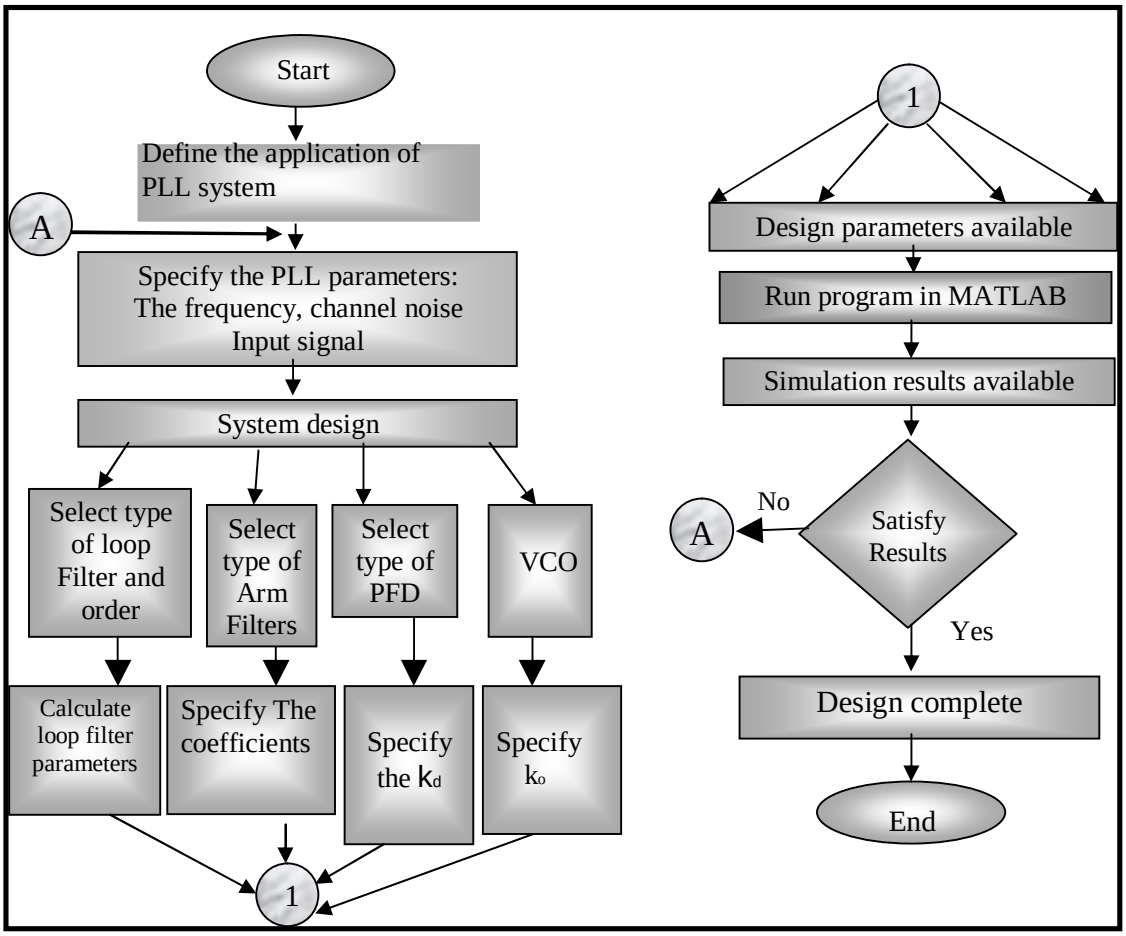

Figure (6): Flow chart of the designed system

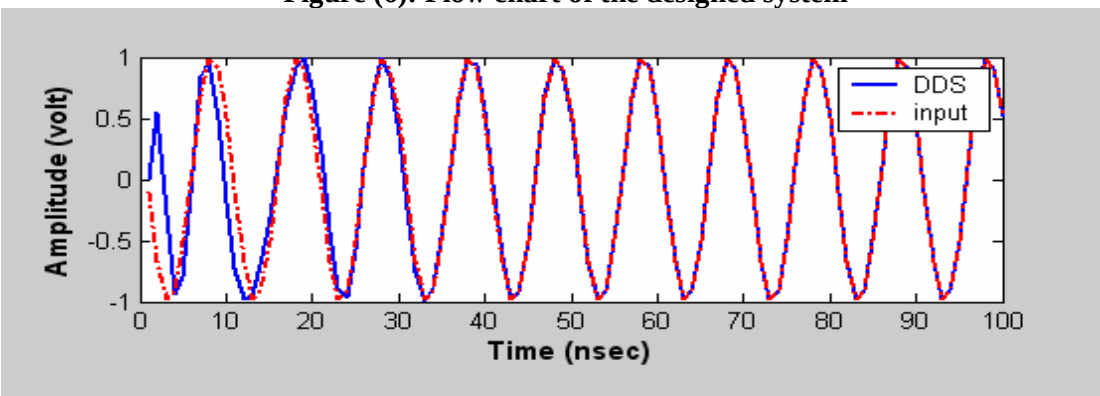

Figure (7) Input and DDS output signals for 10 degree offset case

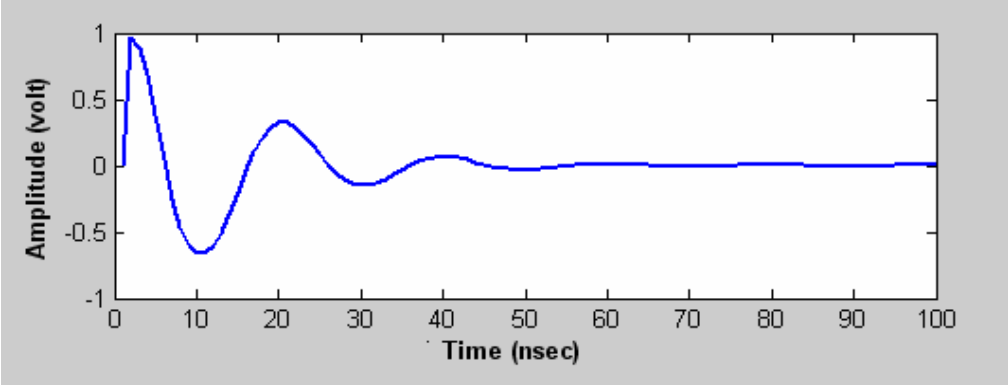

Figure (8) Output loop filter for 10 degree offset case

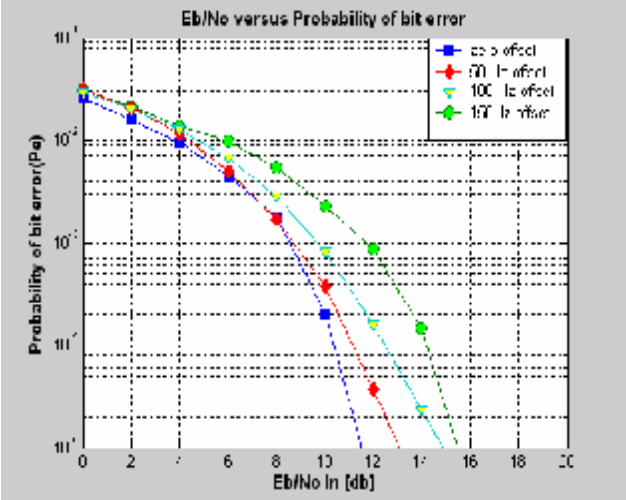

Figure (9): Simulation results of the BPSK signal for frequency offset from 0 to 150 Hz offsets

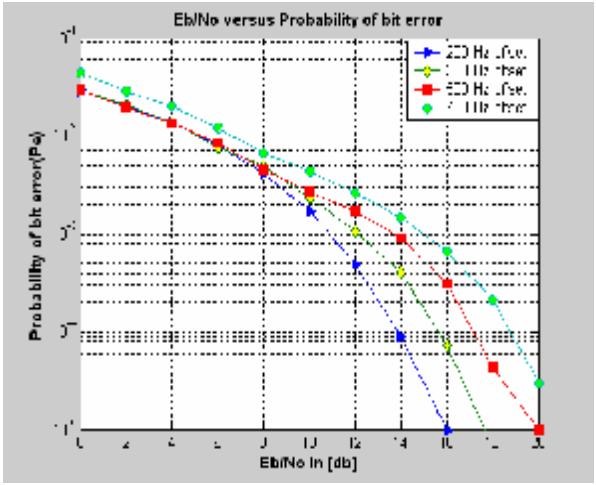

Figure (10): Simulation results of the BPSK signal for frequency offset from 200 to 700 Hz offsets

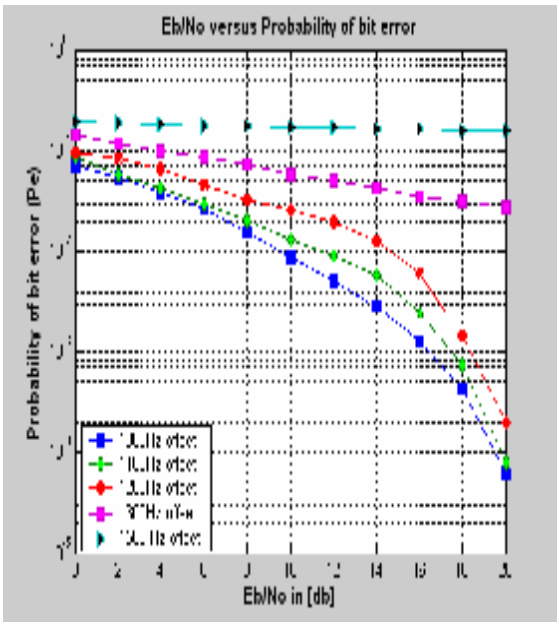

Figure (11): Simulation results of the BPSK signal in the frequency offset from 1000 to 1500 Hz offsets

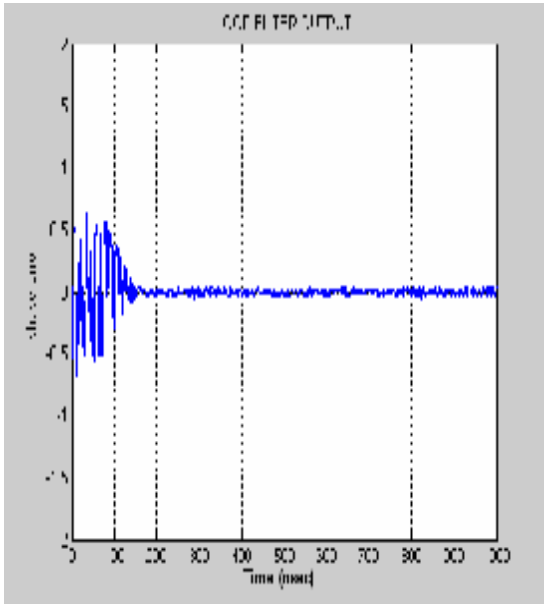

Figure (12): The loop filter output for 100Hz offset

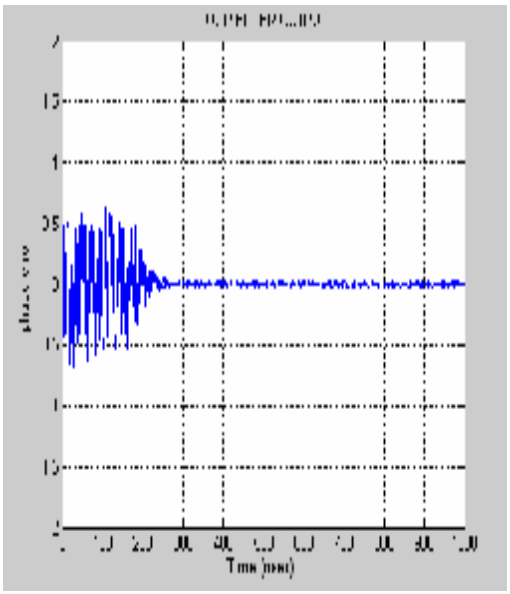

Figure (13): The loop filter output for 300Hz offset

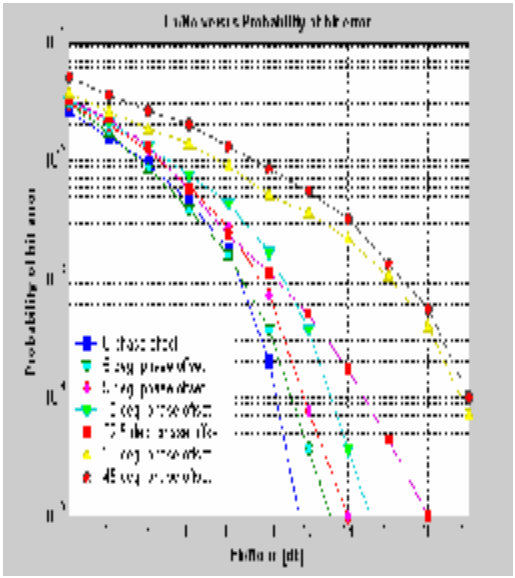

Figure (14) Simulation results of the BPSK signal for zero frequency offset and 0 to 45 deg. Phase offsets

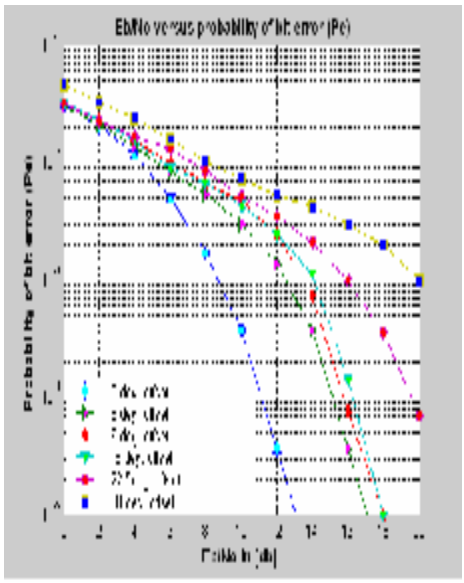

Figure (15) The simulation results of the BPSK when frequency offset is 50Hz and phase offset (0 to 30^{o})

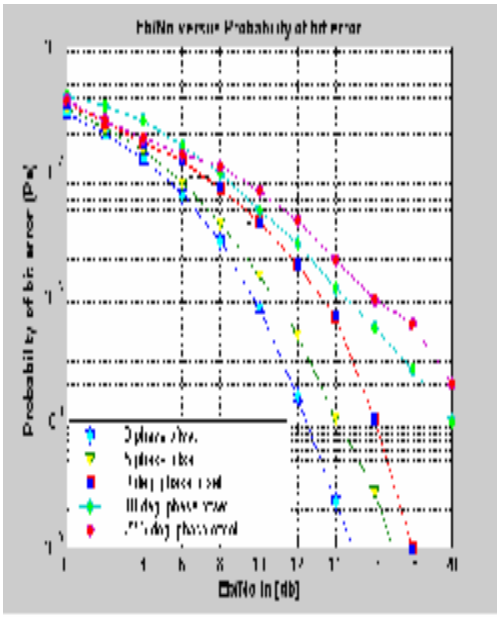

Figure (16) Simulation results of the BPSK when the frequency offset is 100Hz and phase offset(0 to 22.5 deg.)

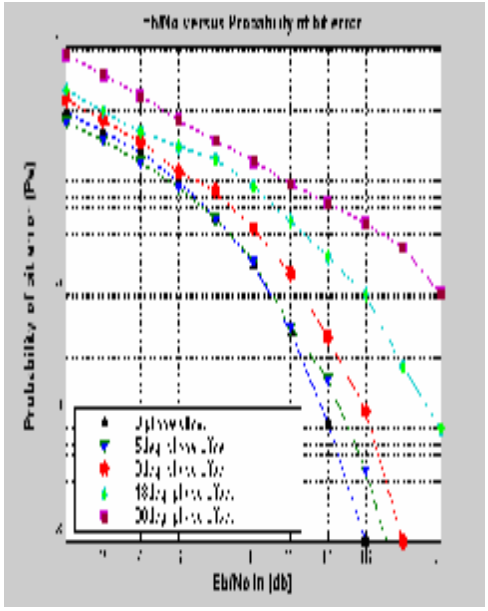

Figure (17) BPSK system has frequency offset is 200Hz and the phase is variable

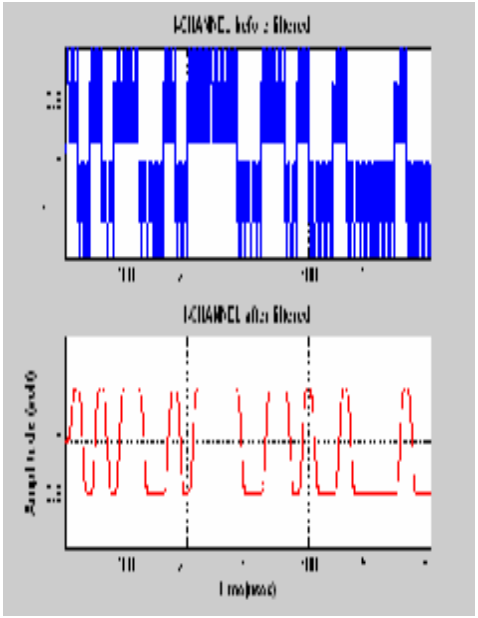

Figure (18) I-channel before and after the filtering action

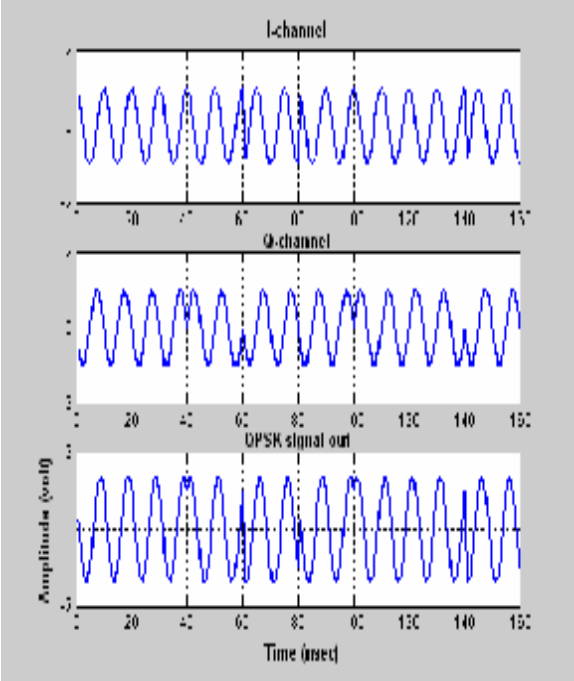

Figure (19) Simulation results of the transmitter of QPSK system

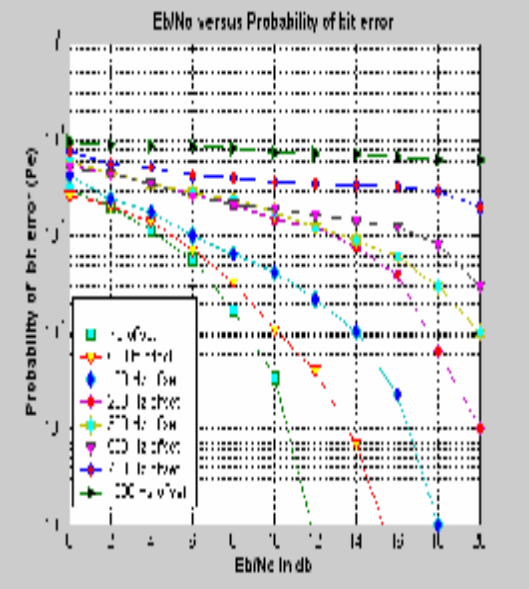

Figure (20) Simulation results of the QPSK system shows the frequency offsets from 0 Hz to 1000Hz

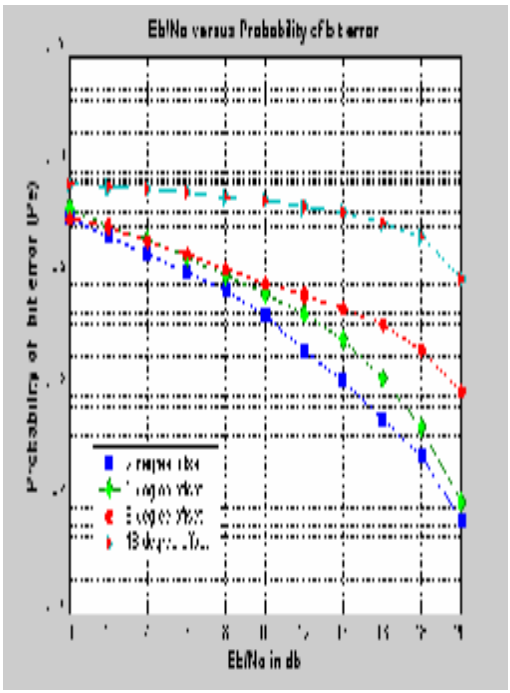

Figure (21) simulation results of the QPSK system shows the phase offsets with no frequency offset

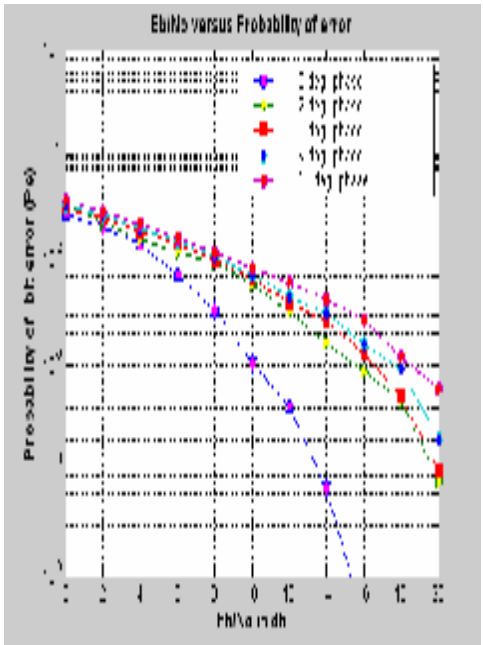

Figure (22) QPSK system have variable phase offset with frequency offset=50Hz