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SWITCHED CAPACITOR FILTER DESIGN SIMULATION

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ABSTRACT - The filter is very important tool in electrical circuits, it is the maen part at communication devices. The design operation of any filter depends upon the frequency, bandwidth and gain. In this paper we will introduce a filter has specialist in design ،easy in change frequency and bandwidth, without need to change the elements of electrical circuit. It is "SC" filters which essentially depend upon the fabrication of (OP AMP) integrated circuit. Here we used (MALAB R2006b) software code to simulate the process of design.

1. INTRODUCTION

The characteristics of all active filters, regardless of architecture, depend on the accuracy of their RC time constants. Because the typical precision achieved for integrated resistors and capacitors is approximately ±30%, a designer is handicapped when attempting to use absolute values for the components in an integrated filter circuit. The ratio of capacitor values on a chip can be accurately controlled . Switched-capacitor filters use these capacitor ratios to achieve precision without the need for precise external components.

The switched-capacitor filter—is an active filter that uses electronic switching of a capacitor to imitate a high-order filter. Several manufacturers produce switched-capacitor filter chips. The filter's cut-off frequency is controlled by a clock frequency applied to the chip, which controls . Typically, the clock frequency is 50–100 times the cutoff frequency of electronic switch the filter [1, 2].

The major advantage of this setup is that the cutoff- frequency is easy to change. So, if the system requires a variable sample rate, the ant aliasing filter can follow along. The major disadvantage is that a switched-capacitor filter is also subject to aliasing [1,2]. Eliminating the aliasing in the switched-capacitor filter sometimes requires a profiler in front of the switched-

capacitor filter and a reconstruction filter behind it. Some switched-capacitor filter chips have an op-amp linear filter onboard the chip to provide pre- or post-filtering. Clock feed through, which is an extraneous signal that switched-capacitor filters create, can occur in the signal. (1.2)

This technique is widespread because it has a few advantages in comparison with other techniques [2.3.4], for instance:

a. The transfer of SC circuits depends not on capacitor values, but on the ratios of them. These ratios can be substantially more accurate than the capacitor values.
b. A clock frequency signal, which is needed for SC circuit operation, can be used for their tuning.
c. SC circuits do not require resistors, whose implementation is difficult in integrated form.

2. The MOS SWITCH

The circuit of MOS switch is shown in figure (1) .

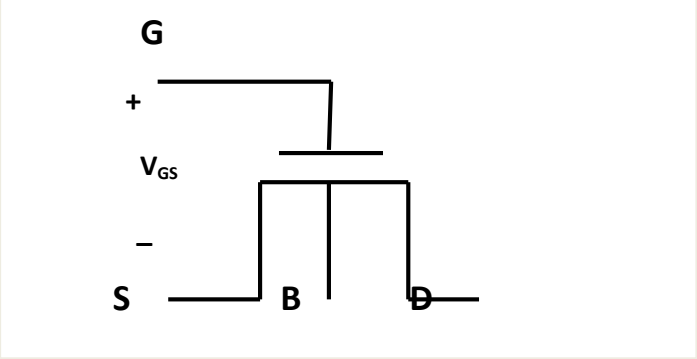

Fig. (1): MOS Transistor.

This transistor can be used as a switch, the voltage between source(S)and gate(G) is either zero ,V_{GS}=0 , so that the transistor is OFF and no current flows, or it is much larger than the threshold voltage V_t ,and the transistor is ON so that current can flow. The path of interest is between source (S) and drain (D), having resistance R_{DS} .When the transistor is in OFF mode, R_{DS} is large (100-1000) MΩ. When the transistor is in ON mode, R_{DS} is much smaller (5-10) KΩ depending on the transistor size; these facts are summarized in the table (1) [4].

Table (1)

condition	state	Equivalent resistor	model
V_{GS}>>vt	ON	10 KΩ	short
V_{GS}< vt	OFF	100 MΩ	open

The switch is open or closed depending on the value of VGS ,open when VGS is low, closed when VGS is high. The voltage waveform that is used to activate the switch can be represented as in the figure (2) below.[4]

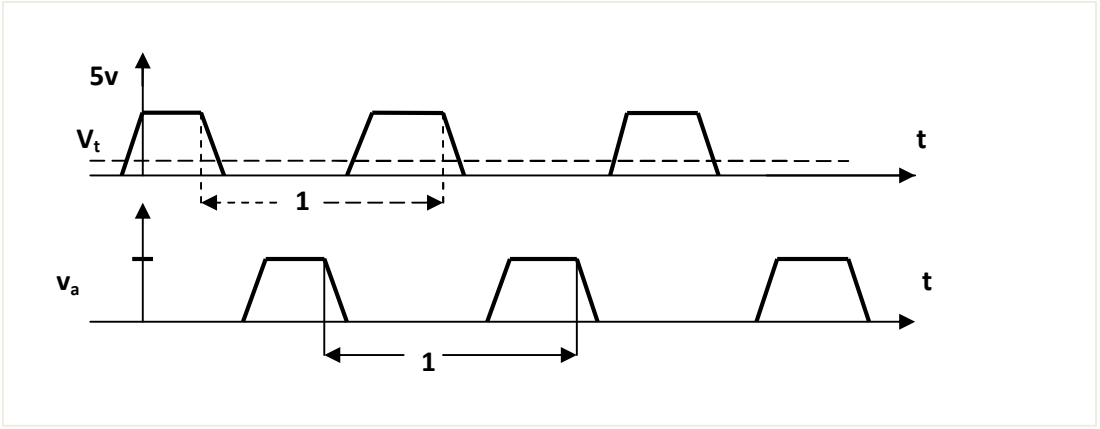

Fig. (2): voltage waveform.

When two MOS switches that are controlled by φ_1 and φ_2 are connected in series as in figure (3).

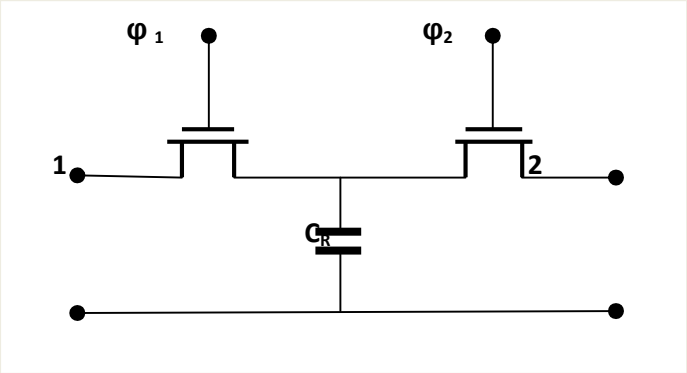

Fig. (3): a capacitor with two MOS switches driven by a two –phase clock.

The capacitor C_R is connected to node 1 during φ_1 (when φ_1 is high) and to node 2 during φ_2 (when φ_2 is high), but at no time are node 1and 2 directly connected through the two switches because one of them is always open. This situation is represented symbolically in figure (4),[(4)].

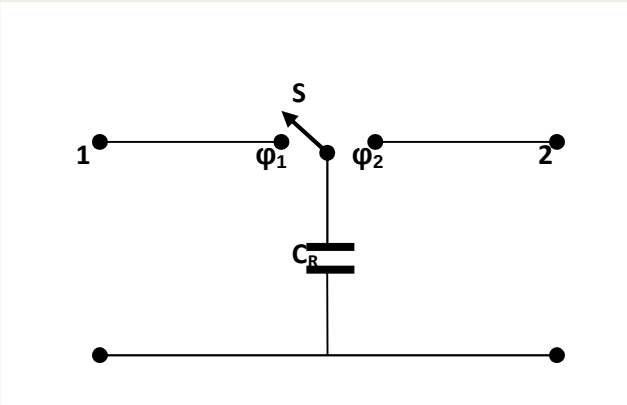

Fig. (4): symbolic representation.

3. THE EQUIVALENT RESISTOR (REQU.).

Consider the extension circuit in figure (5) below:

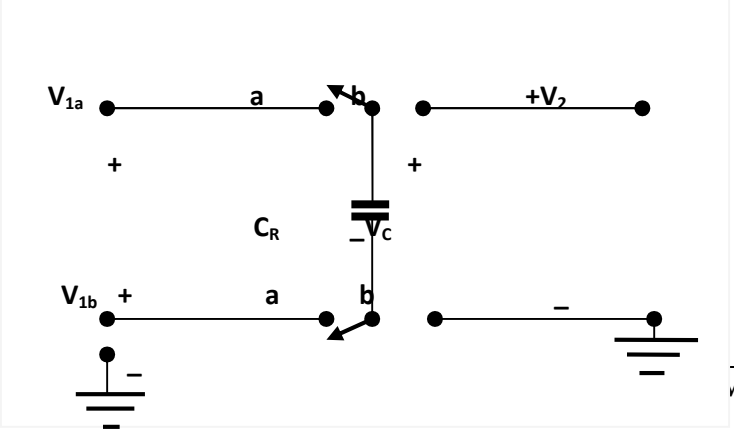

Fig. (5): circuit to form a voltage difference.

Where the capacitor C_R is connected to the voltage (v_1) during phase (φ_1); it is stores the charge (q_1). (4.3)

$$q_1 = C_R v_1 \quad \dots\dots\dots\dots\dots\dots (1)$$

If the connect C_R there after in (φ_2) to the voltage (v_2), the capacitor charge is.

$$q_2 = C_R v_2 \quad \dots\dots\dots\dots\dots\dots (2)$$

The charge transferred from (v_1) to (v_2) is therefore.

$$\Delta q = q_1 - q_2 = C_R(v_1 - v_2) \dots\dots\dots\dots\dots\dots (3)$$

Let the switch(S) be flipped periodically, with clock period (T).such that the clock frequency is:

$$f_c = \frac{1}{T} \dots\dots\dots\dots\dots\dots (4)$$

Is so large compared to the signal frequency ($\omega = 2\pi f$) of the two voltage "sources"(v_1) and (v_2).

$$f_c \gg \omega = 2\pi f \dots\dots\dots\dots\dots\dots (5)$$

That these two signals can be assumed to be constant over the period (T).Since the charge packets get transferred between the two nodes during each clock interval, we can consider the average voltage of the transferred charge packets as a current.(4)

$$i \approx \frac{\Delta q}{T} = \Delta q f_c = f_c C_R (v_1 - v_2) \dots\dots\dots\dots\dots\dots (6)$$

The switched capacitor (SC), behaves approximately like the equivalent resistor.

$$R_{equ.} \approx \frac{v_1 - v_2}{i} = \frac{1}{f_c C_R} \dots\dots\dots\dots\dots\dots (7)$$

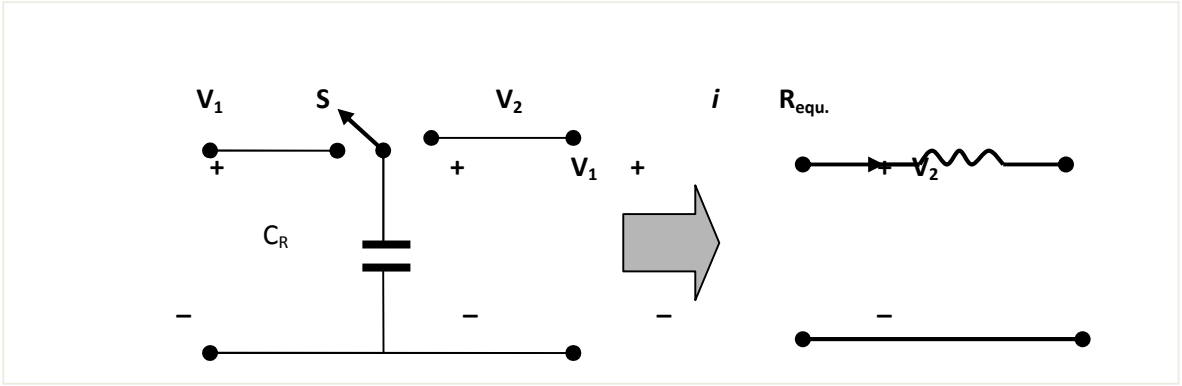

Fig. (6): equivalent Switched-Capacitor Filter circuit.

The "SC" method looks promising for the design of integrated filter at low frequencies, by developing suitable filter circuit. By following the simple equivalence of a resistor and a switched capacitor, take any resistor "R" in the active "RC" filter circuit and replace it by switched capacitor "C_R" and choose a clock frequency "fc" that must be much larger than the signal frequency "fo"[4]

$$C_R = \frac{1}{R f_c} \ldots\ldots\ldots\ldots\ldots\ldots (8)$$

4. FUNDAMENTAL ACTIVE FILTER CIRCUIT.

Consider the integrating summer circuit in figure (7), which it is a fundamental active filter building block.

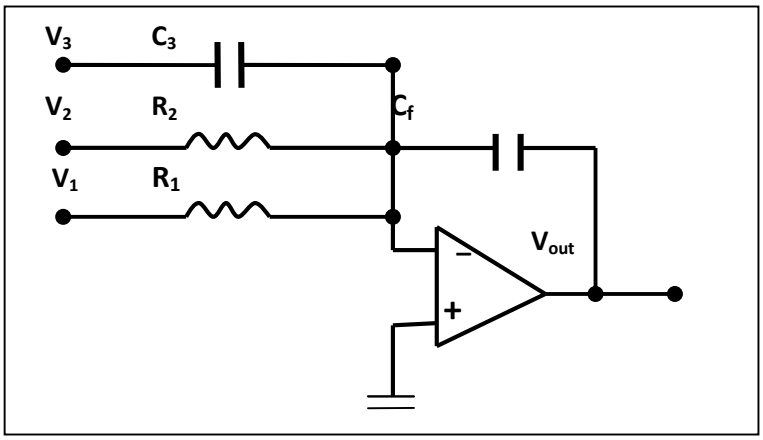

Fig. (7): fundamental active filter building block.

$$V_{out} = \frac{1}{sC_f}(G_1 V_1 + G_2 V_2) - \frac{C_3}{C_f} V_3 \ldots\ldots\ldots\ldots\ldots\ldots (9)$$

Replace the resistor by a switched capacitor that will be.

$$R_1 = \frac{1}{f_c C_1} \equiv G_1 = f_c C_1$$

$$R_2 = \frac{1}{f_c C_2} \equiv G_2 = f_c C_2$$

The circuit will be change to the following form in figure (8).

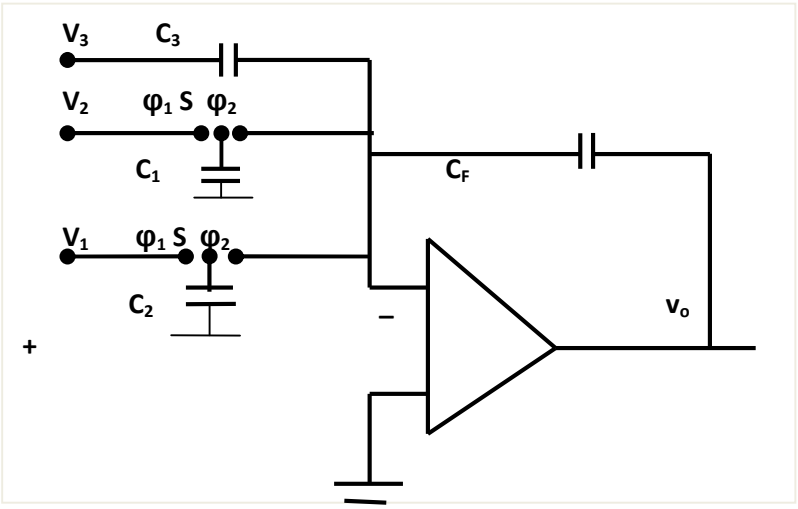

Fig. (8): equivalent circuit.

In this circuit there will be only capacitors.[4]

$$V_{out} = -\frac{f_c}{j\omega C_F}(C_1 V_1 - C_2 V_2) - \frac{C_3}{C_F} V_3 \ldots\ldots\ldots\ldots\ldots\ldots (10)$$

5. SIMULATION OF SC FILTERS CIRCUITE DESIGN.

Let us consider the solution of the following question; construct first order "SC" low pass filter to process the dieference of two voltages "V_1" and "V_2";V_1=2dB;V2=0dB;Fo=4KHZ;Fc=128KHZ;CF=2pF.[4]

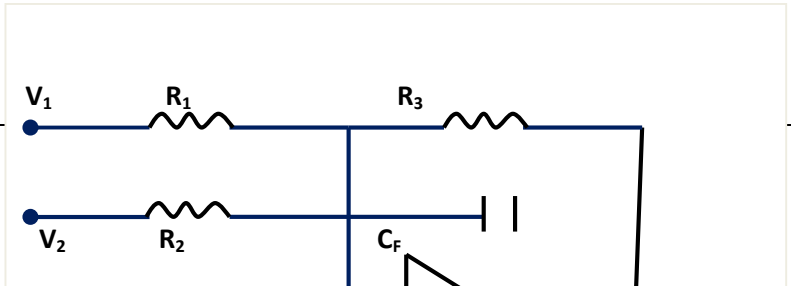

Fig. (9): circuit diagram of above example(1st order low pass filter)**.**

The design based on "RC" and using equation (10) is.

$$V_{out} = -\frac{1}{SC_F + G_3}(V_1 G_1 - V_2 G_2)$$

$$R_3 = \frac{1}{\omega_o C_F} = \frac{1}{2\pi \times 3600 \times 2 \times 10^{-12}}$$

R_3=22.10MΩ

$$\frac{R_3}{R_1} = 1.259(2dB) \; and \; \frac{R_3}{R_2} = 1(0dB)$$

$$R_1 = \frac{R_3}{1.259} = \frac{22.10 \times 10^6}{1.259} = 17.55M\Omega$$

$$R_2 = R_3 = 22.10M\Omega$$

The prescribed clock frequency is 128KHZ; the Switched Capacitors values will be as:

$$C_i = \frac{1}{f_c R_i} \ldots\ldots i = 1,2,3$$

C1=0.445pF C2=0.354pF C3=0.354pF

By using MATLAB software(Appendix A) we find the bode and gain plots for transfer function for different cases of "F_C" and "Fo", (4.3)

6. SIMULATIONS AND RESULTS:

In this section ,three tests are considered .

a. Simulation number one (EXP1).the input value for simulation program was as listed in table (2).

Table (2)

(F_C)	(F_O)	R_1=0.2MΩ	R_2=0.15MΩ	R_3=0.12MΩ
128KHZ	4KHZ	C_1=3.84PF	C_2=5.12PF	C_3=6.41PF

The result of the bode and gain plots are shown in fig.(10).

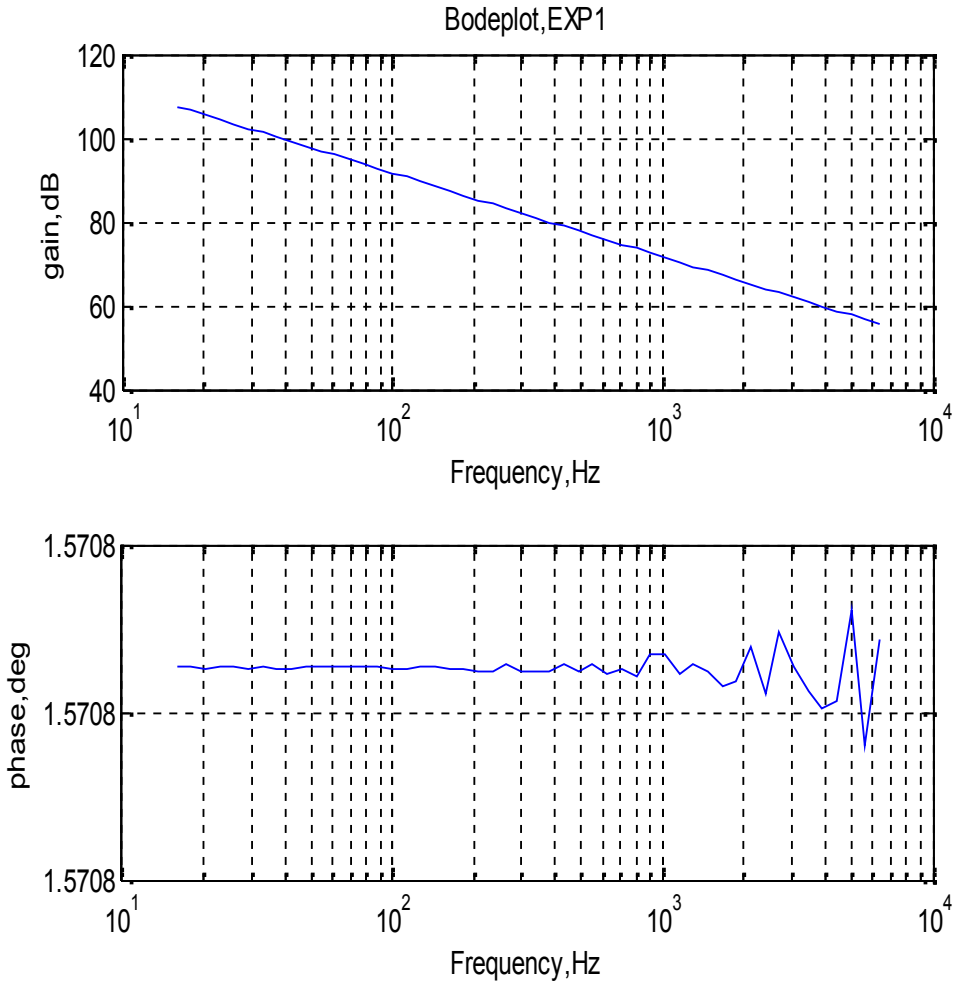

Fig. (10): bode and gain plots for example 1 .

b. Simulation two (EXP2). The input value for simulation program was as listed in table (3).

Table (3)

(FC)	(FO)	R1=17MΩ	R2=13MΩ	R3=2MΩ
120KHZ	3KHZ	C1=4.5e-15F	C2=5.9e-15F	C3=3.8e-014F

The result of the bode and gain plots are illustrated in fig.(11).

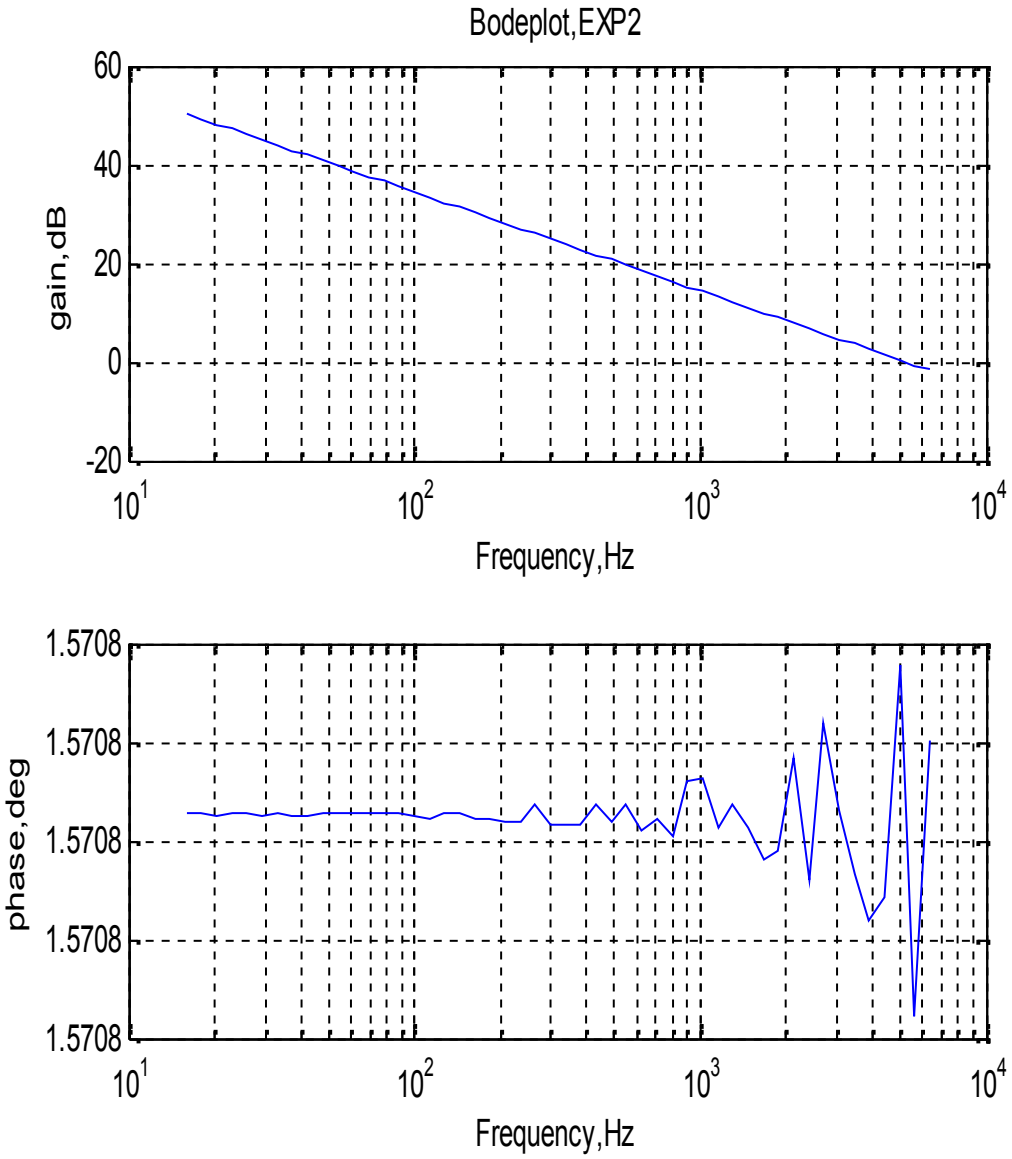

Fig. (11): bode and gain plots for example (2).

c. Simulation three(EXP3).here we fixed the values of R's and C's the changing was only in F_c (clock frequency) and F_o (signal frequency),the result was as shown in the figures (12-16), all selected values was recorded on result figure.

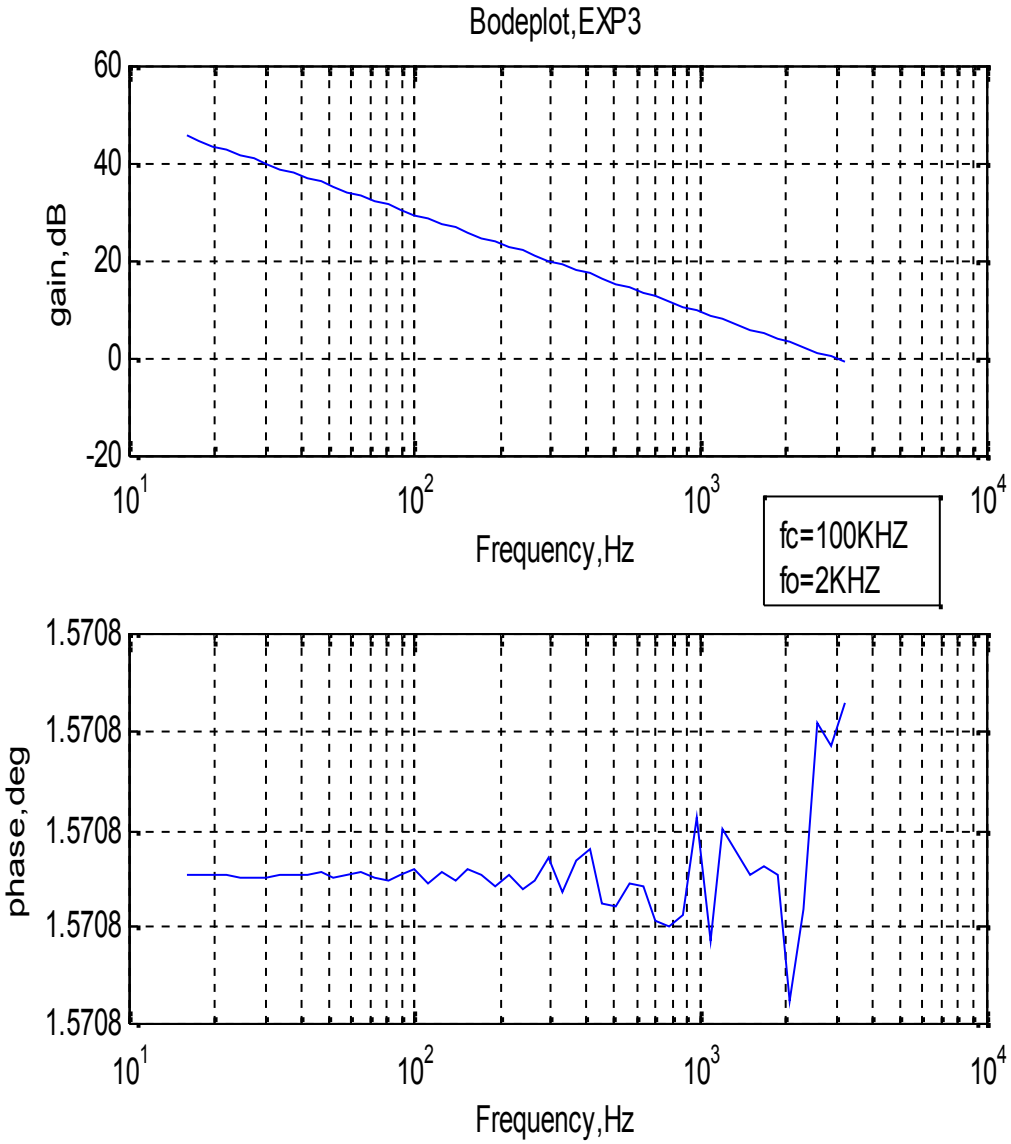

Fig. (12): bode and gain plots for f_c=100khz , f_o=2khz.

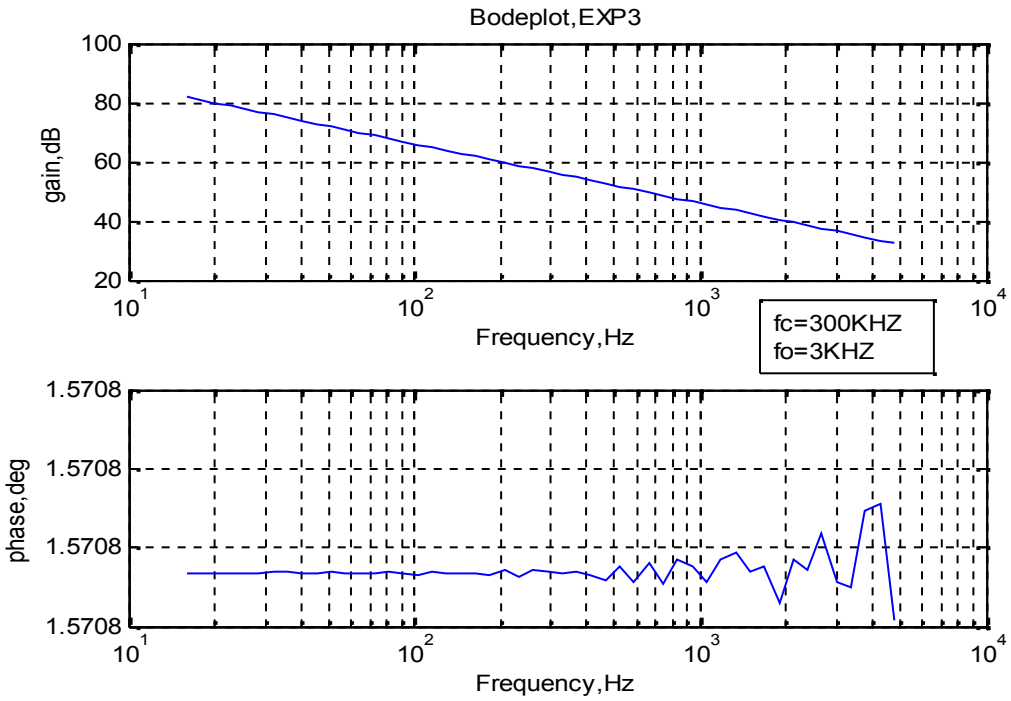

Fig. (13): bode and gain plots for f_c=300khz , f_o=3khz

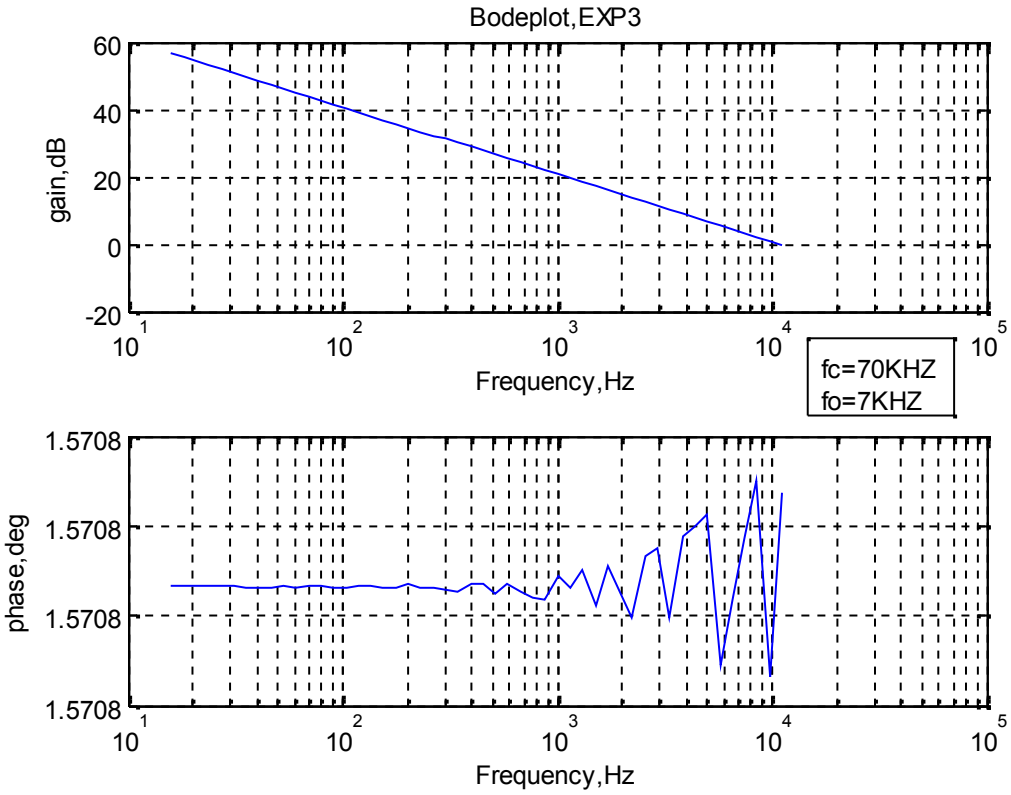

Fig. (14): bode and gain plots for f_c=70khz , f_o=7khz

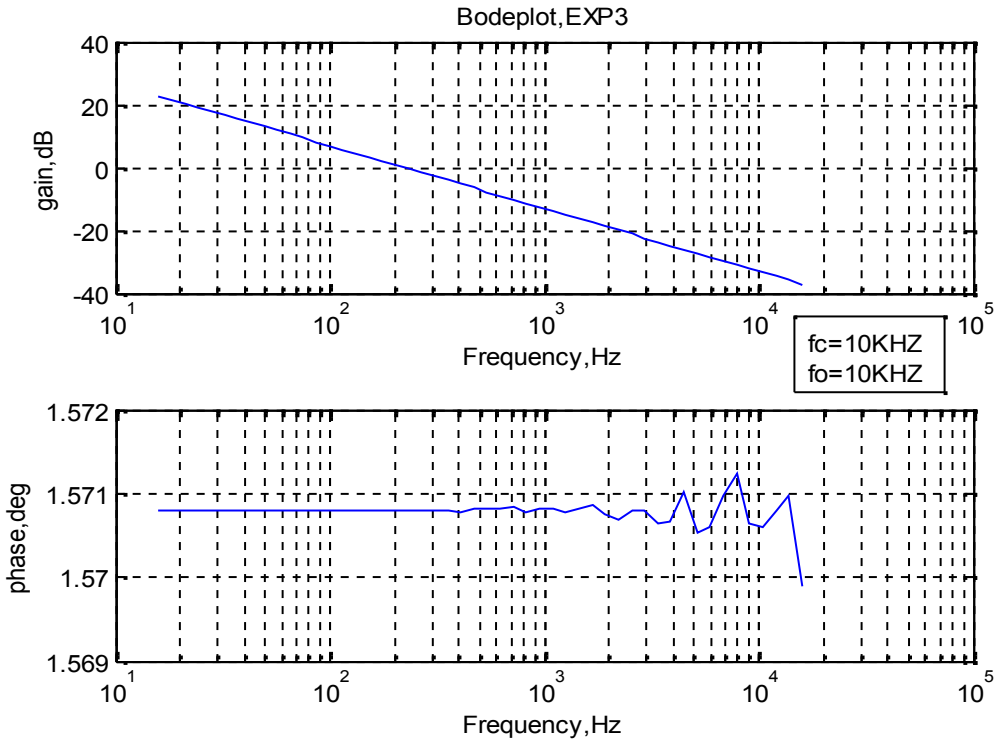

Fig. (15): bode and gain plots for f_c=10khz , f_o=10khz

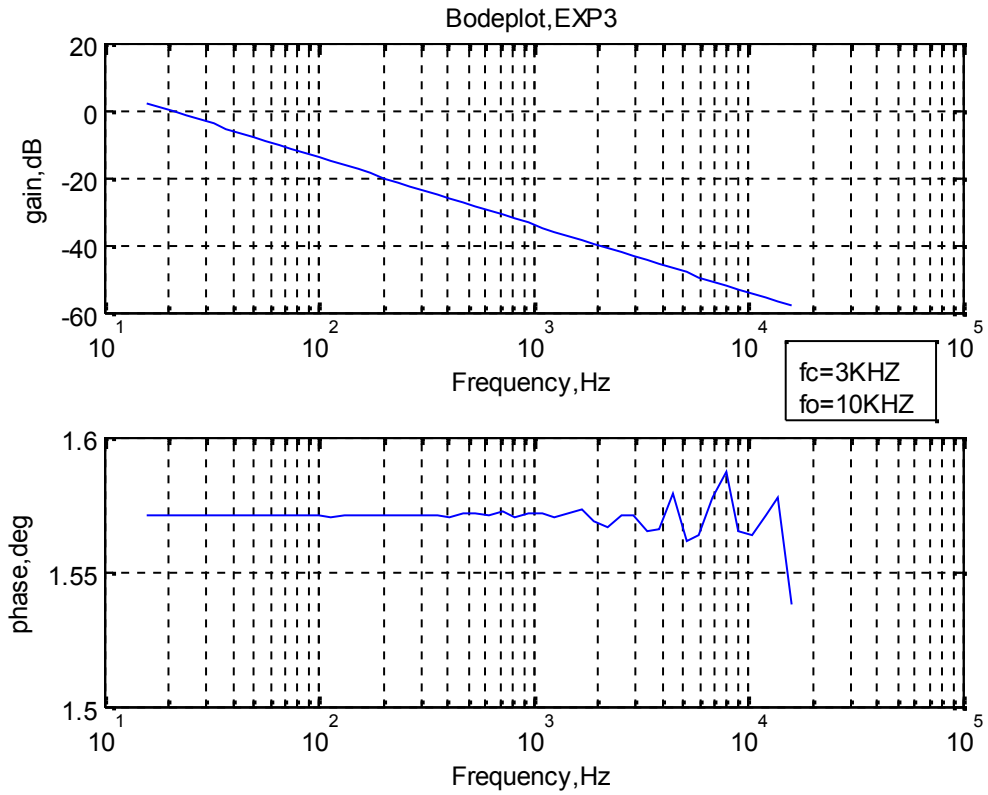

Fig. (16): bode and gain plots for f_c=3khz , f_o=10khz

7. RESULTS AND DISCUSSION

a. Figure (10) represents the simulation of the solution of example; therefore output is ideal low-pass filter output, because the value choose correctively ,the cut-off frequency is clear and the phase curve fluctuation is at 4KHZ.
b. By changing the values of resistors randomly, the result in figure (11) was seem as not good response for the filter and that well indictor to knowledge that filter need more carful .
c. By fixing the values of R's and C's , figure (12) represent the case when F_c=50 F_o , the result is good filter frequency response, we can note the phase fluctuation is exactly at cut-off frequency.
d. Figure (13) represent the case when F_c=100 F_o , so the result is very good ,because the cut-off frequency is at the wanted point.
e. In case $F_c \neq$ (50-100)*F_o figure (14) shows this, this condition is very necessary for operating ,therefore the result is not true and the cut-off frequency is less than 7KHZ .
f. If F_C=F_o the result was very bad as in figure (15),because the two frequencies must be not equal.
g. Finally when F_C< F_o figure (16) shows the result and this is not true according to the condition.

8.CONCLUSION

a. The values of circuit elements depend upon clock frequency.
b. The cut-off frequency vary with the variation of clock frequency.
c. The value of clock frequency must be larger than signal frequency, F_C=(50-100)*F_O, that is very clear in result of exp.3
d. The changing of cutoff frequency did not need change any element in the electrical circuit . only clock frequency must change.
e. The design of such filter did not depending on past design tuning.
f. The value "C_F" is constant and depended upon "MOS" area ,
g. This type of filters is like "RC" active filters.
h. SC circuits are the effect of the features of real operational amplifiers. Which are: finite input resistance, nonzero output resistance, finite slew rate, finite unity-gain bandwidth, and finite voltage gain.

9.REFERENCES

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4. Rolf Schaumamn & Mace Van,"Design of analog filter",Willy&Sons , 2001.

APPENDIX (A)

MATLAB PROGRAM CODE

```
%INPUT DATA%%%%%%%%%%%%%%%%
1-fc=input('  ');%clock frequency
2-fo=input('  ');%signal frequency
3-R1=2*10e6;
4-R2=2.5*10e6;
5-R3=20*10e6;
6-V1=2;
7-V2=1;
%CALAULATION OF CAPACITORS VALUE%%%%%%%%%%%%%%
8-C1=1/(fc*R1)
9-C2=1/(fc*R2)
10-C3=1/(fc*R3)
11-Cf=2*10e-9;
12-wm=100;
13-we=fo;
%TRANSFER FUNCTION CALCULATION%%%%%%%%%%%%%%
14-w=logspace(log10(wm),log10(we));
15-M1=fc*C1*V1;
16-M2=fc*C2*V2;
for n=1:length(w)
    H(n)=-fc/(j*w(n))*fc*(M1+M2)-(C3/Cf)*5*cos(w(n));
    mag(n)=abs(H(n));
    phase(n)=angle(H(n));
end
% PLOT BODE AND GAIN DIAGRAM %%%%%%%%%%
17-subplot(2,1,1);
semilogx(w/(2*pi),20*log10(mag))
```

```
xlabel('Frequency,Hz'),grid on,ylabel('gain,dB'),grid
on,title('Bodeplot,EXP3');
19-subplot(2,1,2),semilogx(w/(2*pi),phase)
xlabel('Frequency,Hz'),grid on,ylabel('phase,deg'),grid on;
```

محاكاة تصميم مرشحة مفتاح سعوي

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مدرس مساعد

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الخلاصة

يعتبر المرشح من الدوائر الالكترونية المهمة جدا ، ويلعب دورا رئيسيا في تركيب أجهزة الاتصالات خصوصا.أن مسألة تصميم المرشح تعتمد على حسابات التردد وعرض الحزمة وكذلك الربح ،وهنا في هذا البحث سوف نقدم مرشح له خصوصية بالتصميم من ناحية سهولة تغيير نطاق الحزمة العاملة دون الحاجة إلى تغيير عناصر الدائرة الالكترونية . انه مرشح(SC) الذي يعتمد بالدرجة الأساسية على صناعة مضخم العمليات نوع (MOS)،وهنا تم تقديم محاكاة باستخدام برنامج (MATLAB-R2006b)،