Design and Implementation of a High Resolution Two Counter Digital Pulse Width Modulation

Jassim K. Hmood*

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Abstract

This paper presents a high resolution Digital Pulse Width Modulation "DPWM" for the voltage regulator application. The PWM signal is generated by using two fast clock counters. In this approach, the pulse width is combined from two parts depending on two counter schemes. MSBs of the DPWM generates first part of pulse that achieved by a first counter-phase comparator scheme, and the LSBs of the DPWM generates second part of pulse that obtained through a second counter- phase comparator scheme. The resolution of present pulse width depends on the resolution of second counter.

The developed pulse width modulator has high precision, good linearity, and wide duty cycle range. Further, it can be flexibly reconfigured for multi-phase PWM operation with no restriction on duty cycle range. In this work, a 714 kHz switching frequency DPWM module with 9- bit resolution is tested by simulation program.

Keywords: Pulse width modulation, voltage regulator, counters, buck converter.

تصميم وتنفيذ مضمن عرض نبضة رقمي ذو ثبات عالي باستخدام عدادين

الخلاصة

في هذا البحث نقدم تضمين لعرض نبضة رقمي عالي الثبات يستخدم لتطبيقات منظمات الفولتيـــة. تـــم توليد إشارة المضمن باستخدام عدادين سريعين. أما عرض النبضة فيتركب مـــن جـــزأين بالاعتمـــاد علـــى محتوى العدادين. القيمة العظمى للمضمن تولد الجزء الأول من النبضة والذي يتحقق بواســـطة أول مخطـــط عداد - مقارن الطور. أما القيمة الدنيا للمضمن فتولد الجزء الثاني من النبضة والـــذي يُحـــرز مـــن خـــلال المخطط الثاني للعداد - مقارن الطور.

أن مضمن عرض النبضة المطور يملك مواصفات منها:أنه بالغ الدقة و ذو خطية جيدة و مدى واســـع لتغيير دورة الاشتغال. علاوة على ذلك, فانه مرن الاستخدام في مضمن عرض النبضة متعدد الطور بدون تقييد في مدى دورة الاشتغال. في هذا العمل فُحصَ مضمن عرض النبضة رقمي ذو ثبات بمقـــدار 9-bit ويعمل بتردد 714kHz باستخدام برنامج تظاهر.

1. Introduction

In recent years, the interest on digital control for switching power converters has grown considerably. When compared to its analog counterpart, the digital control approach has the potential to offer several advantages, such as the immunity to component variations, communication capability, the ability to perform sophisticated control algorithms and self-calibrations [1].

This paper discuses the design and implement the high-resolution digital pulse width modulation DPWM used to digitally controlled PWM converters. Section 2, gives an overview of the structure of digital PWM controllers. In Section 3, design challenge of DPWM is

* Laser and Optoelectronic Engineering Department, University of Technology / Baghdad

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2412-0758/University of Technology-Iraq, Baghdad, Iraq

introduced. Then, proposed two-counter DPWM scheme is investigated in Section 4. In Section 5, some experimental results verify proposed concept. The summary of paper and present conclusions discussed in Section 6.

2. Overview of the structure of DPWM

The digital pulse width modulation can be done by applying the conventional analog ramp-comparator pulse -width modulation scheme in the digital domain. A digital pulse width modulator is constructed by using a fast-clocked counter, which served as the function of a digital ramp, and a digital comparator. The resolution of the pulse width in time domain is determined by the clock period. A clock with frequency $2^n fs$ is needed to achieve n-bit resolution for a given switching frequency of *fs*.

A tapped delay-line DPWM and a similar ring oscillator MUX DPWM scheme as developed in [2] circumvent the high-frequency clock requirement. In either case, the delay line or the ring oscillator only runs at the converter switching frequency and fine resolution is achieved by multiplexing a particular tap to the output, according to the duty cycle command. Power consumption is significantly reduced compared to the conventional counter-based structure. However, this approach requires a large-size multiplexer and a large-size delay line or ring oscillator in order to achieve high resolution.

A hybrid scheme based on combining the conventional counter-based and ring-oscillator- MUX has been reported in [3-5]. In this approach, the MSBs of the DPWM resolution are achieved by a conventional counter-based scheme, and the LSBs of the DPWM resolution are obtained through a ring-oscillator-MUX scheme the area and routing complexity. In the hybrid scheme, the resolution of the DPWM is limited by the pulse width of the non-overlapping pulses generated by the delay cell. Therefore, it is difficult to achieve sub-nanosecond resolution.

The present digital pulse-width modulation scheme is based on combining the two counters. In this approach, the MSBs of the DPWM determine the pulse width of first part by a first counter scheme. In same time, the LSBs of the DPWM resolution are obtained through another counter scheme. This approach permits the fast clock requirement and reduces the power consumption significantly compared to the conventional counter-based structure. Compared to the ring oscillator-MUX scheme, this approach reduces the area and routing complexity. In the present scheme, the resolution of the DPWM in time domain is determined by the clock period.

The digital pulse width modulator (DPWM) module takes the duty ratio command and the SR timing as inputs and converts this data into DPWM and SR signals that control the high side and low side switches.

In this work, a 714 kHz switching frequency DPWM module with 9- bit resolution is implemented based on a two counter approach. The first part of pulse is generated depending on five MSB by using the first counter and four LSB is generating the second part by the second counter. The resolution of present pulse width depends on the resolution of second counter. The second counters are running at same master clock frequency. A DPWM scheme is proposed to improve resolution while keeping relative low cost.

3. Design Challenge of DPWM

Fig.(1) illustrates the structure of a buck converter with voltage-mode digital control, where the digital pulse-width modulator (DPWM) and the analog-to-

digital converter (ADC) serve as the interfaces between the analog power stage and the digital controller.

Because of the inherent digital characteristics, there exist quantization effects in the DPWM and the ADC only discrete values are obtained at their outputs. As the result of the quantization effect of the DPWM, only limited resolution of the duty cycle, *D*, can be obtained. Consequently, the output voltage also has limited resolution, V_{o_DPWM}: [1]

$$DV_{o\_DPWM} = Vin \times DD$$

It has been observed and analyzed that a large-magnitude limit-cycle oscillation might happen at the output voltage if V_{o_DPWM} is not as fine as that of the ADC, V_{ADC}, i.e.,[1]

$$DV_{o\_DPWM} > DV_{ADC}$$

This limit-cycle oscillation is a severe concern for switching power converters, especially for the application requiring tight output regulation as shown in Fig.(2).

The first step towards eliminating limit cycles is to ensure there is a DPWM level that maps into the zero-error bin. This can be guaranteed if the resolution of the DPWM module is finer than the resolution of the ADC. A one-bit difference in the resolutions, $N_{DPWM} = N_{ADC} + 1$, seems sufficient in most applications since it provides two DPWM levels per one ADC level [6].

Another challenge to the DPWM design comes from the converter switching frequency because the duty cycle resolution is determined by:

$$DD = t_{clock} \times f_s$$

Where t_{clock} is the digital controller's system clock cycle, and f_s is the converter switching frequency. To obtain the same V_{o_DPWM} to avoid the limit-cycle oscillation, a higher switching frequency converter demands a faster digital controller system clock, which also poses stringent challenges on the DPWM design.

4. Proposed Two-Counter Digital PWM Scheme

A 9-bit two-counter DPWM is illustrated in Fig.(3). The rising edge of the PWM signal is generated by a fixed clock signal and the falling edge is generated by combining a 5-bit and another 4-bit counter - phase comparator schemes. The clock generator runs at the frequency of 100MHz, and the 5-bit counter divides the switching period into 8 segments. In each segment, the 4-bit counter generates pulse width according to load data (maximum pulse width equal to t_s /8). The rising edge of the PWM signal is generated at the beginning of the switching cycle. The falling edge of the PWM signal is generated from the 4-bit counter, which is specified by the counter according to the 4-LSB of the duty cycle command, after the counter reaches the count corresponding to the 5-MSB's of the duty cycle command.

The frequency divider counter is consisting of 6-bit loading down counter. The frequency divider counter is used to generate the switching frequency f_s. The beginning of the switching cycle is obtained by the beginning of the switching frequency. Then the rising edge of PWM is determined by the beginning of frequency divider counter.

The duty ratio command is divided into two parts the 5-MSB is loaded to the counter No.1 and 4- LSB is loaded to the counter No.2. During each modulation cycle, the 5-MSB is loaded to the counter No.1. Then the counter is driven down by a clock signal f_{clock} with a frequency given by:

$$f_{clock} = 2^N \times fs$$

where, N is the counter number of bits

After the counter reaches its zero value, a low-level output pulse (terminal count down TCD) is generated to indicate the counter under flows. The TCD1 pulse, which is used to reset the flip-flop No.1, remains at its low state until the next modulation cycle starts as shown in Fig.(4). Thus, the pulse width of first part is obtained by setting the flip-flop into high state at the start of each modulation period, and after a period dependent on the content of the 5-bit counter, the flip-flop is rest into the low state. As shown in Fig.(3), the inverted output of flip-flop No.1 is control the start count of the 4-bit counter. The 4-bit counter is begin count down when the 5-bit counter is terminate count down and the output of flip flop No.1 is low state. After the counter reaches its zero value, a low-level output pulse (terminal count down TCD) is generated to indicate the counter under flows. The TCD pulse, which is used to reset the flip-flop No.2, remains at its low state until the next modulation cycle starts. Thus, the pulse width of first part is obtained by setting the flip-flop into high state at the start of each modulation period, and after a period dependent on the content of the 4-bit counter, the flip-flop is rest into the low state. The output of flip flop No.2 is consider the output of DPWM because the flip flop is used to combine the 5-bit counter and 4-bit counter outputs

Fig.(5) shows the block diagram for generating the synchronous rectifier (SR) control signal with programmable deadtime and its corresponding switching waveform. The synchronous rectifier has a complementary switching pattern with deadtime td_{on} and td_{off} relative to the rising and falling edges of the PWM signal. The same circuit used to generate PWM signal is used here to generate the rising edge and falling edge of the SR control signal respectively with duty cycle input $D + td_{off}$ and $T - td_{on}$ respectively. A falling edge triggered set-reset flip-flop is used to combine the two signals to generate the SR control signal. The deadtime td_{on} and td_{off} are stored in registers and can be programmed externally through a serial parallel interface or internally with a deadtime look up table [7].

5. Experimental Results

To verify the proposed DPWM scheme, the circuit-maker simulation program was used. This program utilizes a XSPICE simulation program to analyze the electronic circuits. The digital pulse width modulator is implemented by using programmable binary counters, D-flip flops, AND gate, data sequencer blocks, and clock generator.

Figure (6) shows the time domain response of the modulator to a triangle input voltage command V_{in} without duty cycle saturation. When applying a large triangle voltage command V_{in} at the input and forcing the duty cycle of the PWM signal from zero to 100%, the PWM signal was transferred from segment to another as shown in Fig(7). Fig.(8) gives the measured output PWM duty ratio versus input voltage command V_{in}, showing the good linearity of the pulse width modulator. The modulation characteristic is verified by applying a large step voltage at the input. A positive step input voltage results a 24% duty cycle. When, the positive voltage command increase immediately, the duty cycle will increased immediately as shown in Fig.(9,a). Figure (9,b) shows the PWM signal when the input voltage change from certain input voltage command to lower input voltage command. The duty cycle is change from 60% to 12% immediately. As seen, single edge of the PWM signal is modulated by

the input voltage and the designed pulse-width modulator provides fast transient response.

6. Conclusion

In this paper, high resolution digital pulse width modulation scheme has been demonstrated. Some of the technical challenges of implementing digital Pulse width modulation are introduced. The two-counter DPWM scheme is proposed with relative low frequency clock, a much higher equivalent frequency.

A new, segmented DPWM architecture is aiming to achieve good resolution by segmentation of the input digital code to drive programmable binary counters. A simulation proof of concept design case consisting of a 9-bit DPWM circuit operating at 714 kHz switching frequency, is described, and simulation results are shown to validate its functionality

The falling edge of the PWM signal is controlled by the instantaneous input voltage. The fast transient response, good linearity, low power, and low cost make it an attractive pulse-width modulator candidate for integrated power management ICs

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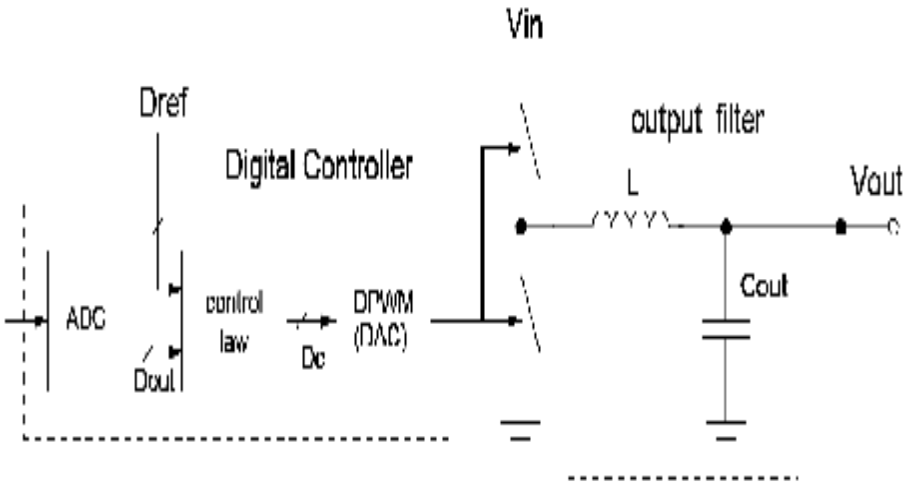


Figure.(1) Block diagram of a digitally controlled PWM converter

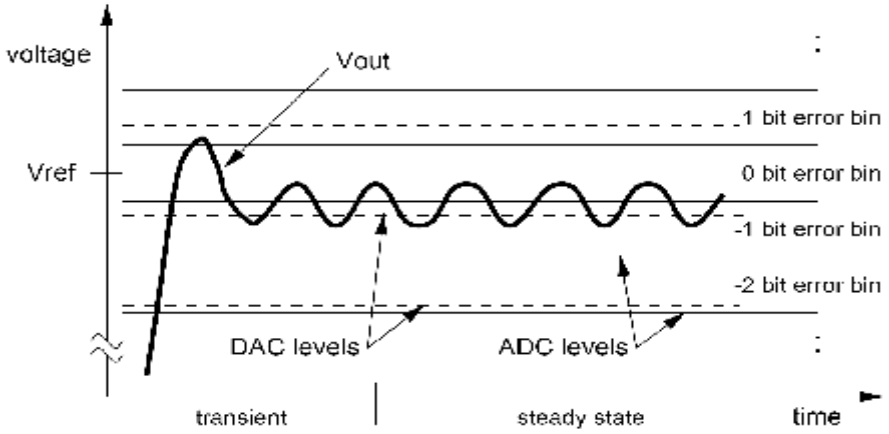


Figure (2) Limit cycle oscillation with insufficient DPWM resolution

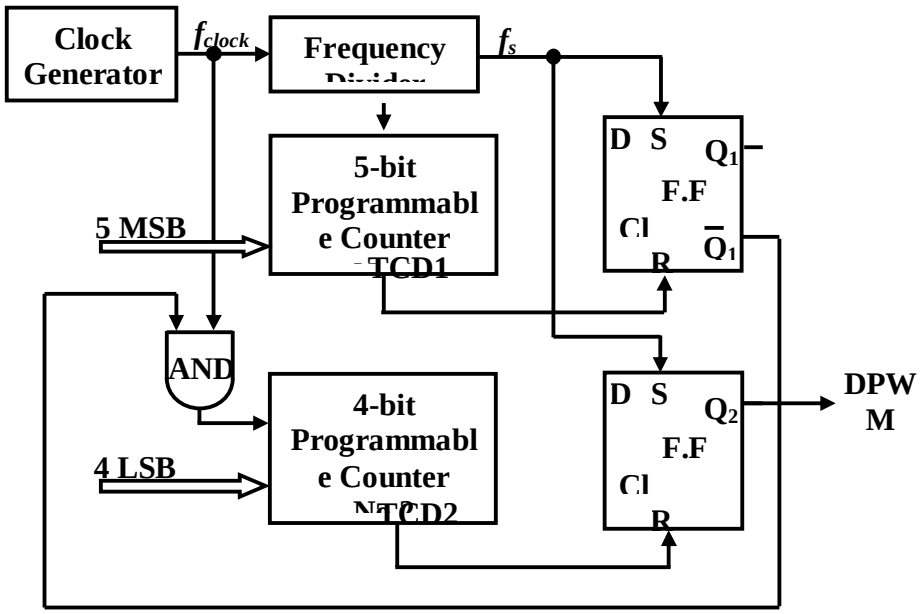


Figure (3) Block diagram of proposed DPWM

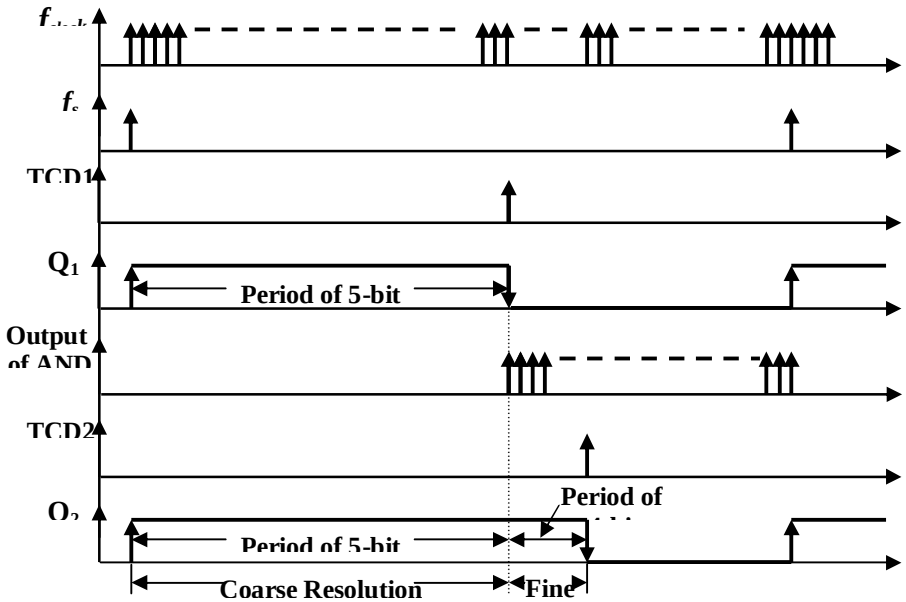


Figure.(4) Illustrate the timing diagram of the two

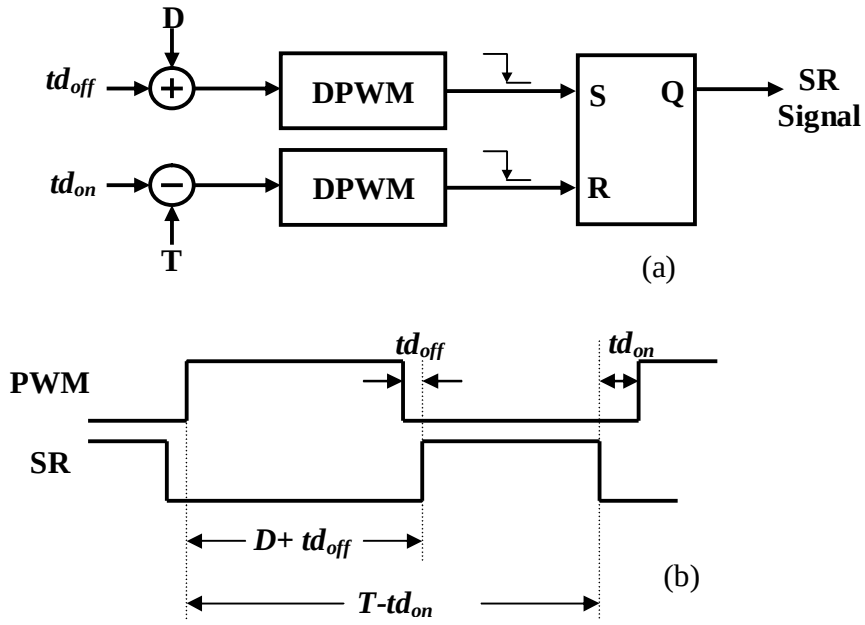


Figure (5) Synchronous rectifier control signal generation (a) Block

Figure.(6) The time domain response of the modulator to a triangle input voltage without duty ratio saturation.

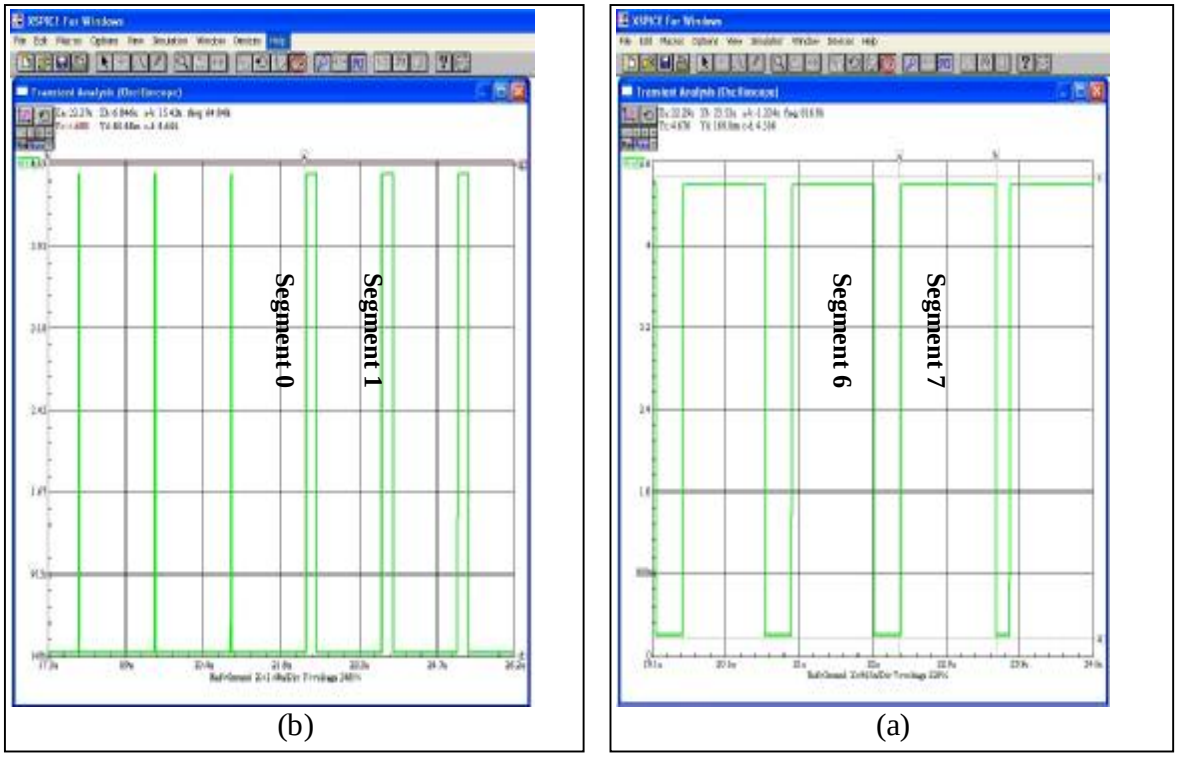


Figure.(7) Illustrate the transition of PWM signal from segment to another

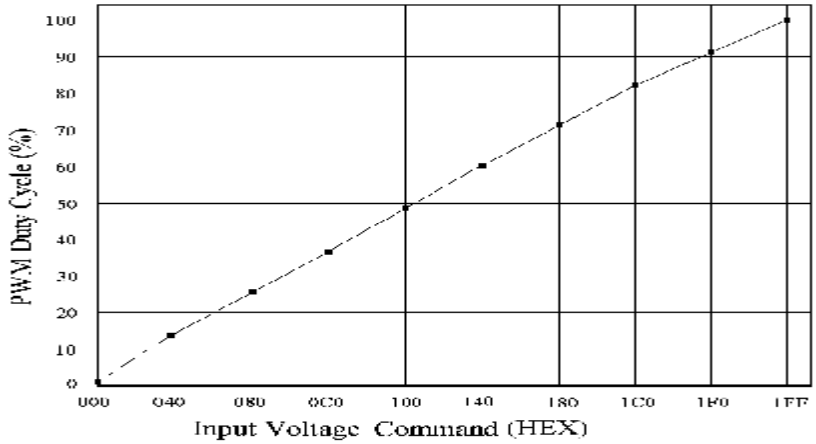
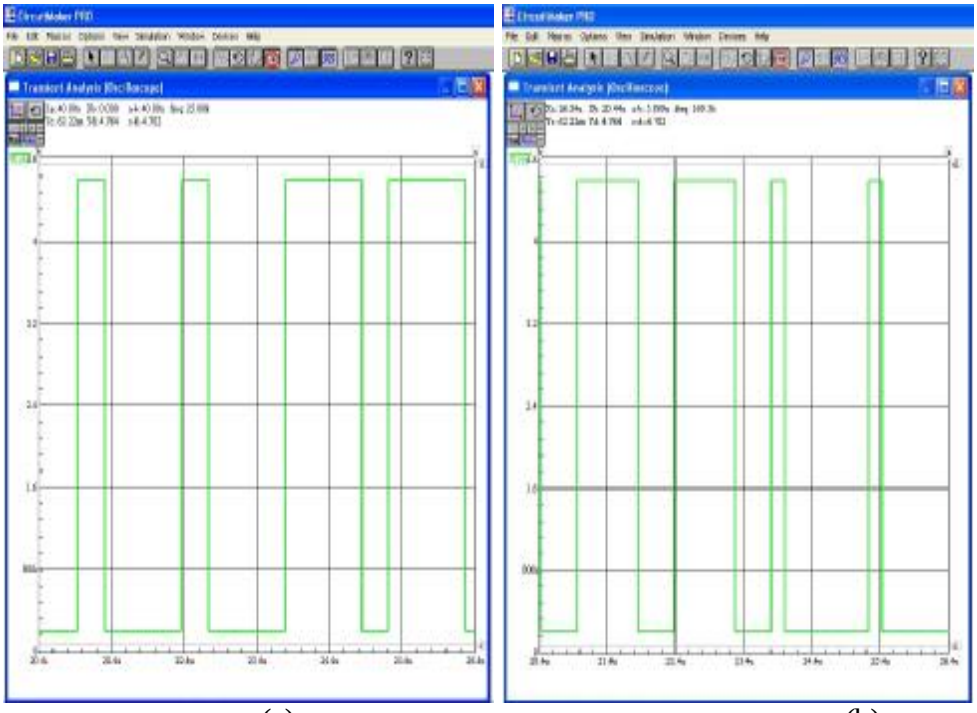


Figure.(8) Measured Transfer Characteristic of PWM duty ratio versus input voltage command.



(a) (b)

Figure.(9) Experimental transient response of pulse width modulate
(a) Applying step up voltage at input
(b) Applying step down voltage at input