Efficient Implementation of Serial Search Synchronization Sub-system for Direct Sequence Spread Spectrum System Using FPGA

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Abstract

A complete synchronization / detection sub-system for direct sequence spread spectrum (DS/SS) system has been designed and implemented using Xilinx-Virtex Field Programmable Gate Array (FPGA) device. Then, a number of modifications has been made to the original sub-system to obtain optimum FPGA cost / delay optimization. For this purpose, the 8 bit representation of BPSK DS/SS signal was replaced by only one bit representation with the same performance at middle values of signal-to-noise ratio. The synthesis and implementation reports of VHDL programs that written to model both systems are developed for comparison purpose. These reports show that the modified implementation offers a cost reduction factor of 95.8% and delay reduction factor of 50% as compared with the traditional one.

بناء كفوء لمنظومة تزامن البحث المتوالي لنظام الطيف المنتشر بالمتتابعة المباشرة باستخدام مصفوفة البوابات المبرمجة الواسعة

الخلاصة

في هذا البحث تم تصميم وبناء منظومة سيطرة التزامن لنظام اتصالات الطيف المنتشر بالمتتابعة المباشرة باستخدام تقنية مصفوفة البوابات المبرمجة الواسعة نوع Xilinx-Virtex بعد ذلك تم تطوير التصميم المذكور أعلاه ليحقق توازن مثالي مابين سرعة المنظومة و مقدار كلفتها. ولأجل هذا الغرض ، تم تمثيل كل عينة في أشارة الطيف المنتشر المضمنة بالطور الثنائي باستخدام بت واحدة فقط عوضاً عن التمثيل بثمانية بتات وبما يحقق نفس الأداء لقيم متوسطة لقدرة الأشارة الى الضوضاء. ولأجل المقارنة بين التصميمين ، تم الأستفادة من تقارير البناء و التركيب الخاصة ببرامج الـ VHDL الخاصة بمكونات النظامين. تلك التقارير بينت بأن التصميم المطور يمتلك كلفة أقل بمقدار ٩٥,٨% وتأخير زمني أقل بمقدار ٥٠% مقارنة بالتصميم الأصلي.

I. Introduction:

Direct sequence spread spectrum (DS/SS) is the most common version of spread spectrum system in use today, due its simplicity and ease of implementation [1-3]. In this technique, the input data is directly modulated by a wideband Pseudo Noise (PN) sequence. In order to demodulate the received DS signal, it must be despeaded first by multiplication with a locally generated PN code replica. The local PN sequence must be in perfect synchronism with the received PN sequence. This is done in two steps, the first is the acquisition process, and the second is the tracking.

One of the well known acquisition schemes for DS/SS system is the serial search acquisition. It is widely used due to its ability to operate at low values of signal-to-noise ratio. The synchronization system of DS/SS receiver can be implemented using three different methods: firstly, using special programmable devices like multipliers, programmable filters and one chip code generators. Secondly, using processors such as microprocessor, microcomputer

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or TMS with suitable software. Thirdly, using the programmable devices such as Field Programmable Gate Array FPGA. The last approach is regarded as a complex method which requires the designing of all components in a form suitable for the architecture of the base devices. This approach is economical, flexible and easy in implementation in comparison with the first approach and provides high speed in comparison with the second approach. It is suitable for real time applications for speed less than 100 Million Cycle Per Second (MCPS).

The FPGA design performance measures are the cost and the speed. The design is said to be optimal when it has minimum cost and maximum speed (minimum delay). The cost of FPGA is measured by the number of cells that the design consume while the speed is measured by the maximum number of delay units that are consumed until the output is obtained. The performance of FPGA design is optimized by rewriting the logic expressions that describes the building units until suitable formulation is obtained.

In this paper, a new serial search synchronization scheme with data modulation (well known problem in DS/SS synchronization systems) is proposed for efficient implementation using FPGA devices. VHDL programs are written to implement each component of the implemented scheme. The synthesis reports of cost, delay and other parameters are obtained from ISE4.1a package.

II. FPGA Implementation of traditional serial search synchronization / detection scheme :

A DS/SS transmitter is implemented first to generate DS/SS signal. The transmitted data are assumed to alternating with 100 KHz rate (clk0). The PN code length is 127 chip with 1 MHz chip rate (clk1). Since the FPGA implementation requires fully digital environments, the DS/SS signal is transmitted as 8 bit symbols at 6 MHz clock frequency (clk2). The local code generator at the receiver side is shown in Fig.1. The local code generator produces two signals: BPSK modulated PN sequence (lc) and BPSK modulated PN sequence with alternating data (dc). Assuming that both transmitted data and locally generated one have the same boundary locations relative to the spreading code. Therefore, correlating the transmitted signal with the two locally generated ones using two isolated branches would result in correlation power at least in one of them. This arrangement is proposed to solve the problem of data presence during acquisition process.

Fig.2 illustrates the serial search synchronization acquisition scheme with data modulation. This detector performs two operations: extract output data from received signal (denoted as rx) and compute powers resulting from correlating the received and the locally generated signals, and compare them with preset thresholds to declare signal presence. The two correlation processes are performed over fixed time intervals (correlation time: 30 chips). The integration results are compared with two thresholds (Vth_1 and Vth_2), one of them (Vth_1) is to decide acquisition presence while the other (Vth_2) is to declare tracking presence. If Vth_1 is not crossed, the local code generator is delayed by a number of samples equivalent to the time interval $T_c/2$ where T_c is the duration of the PN sequence bit (Acquisition decision signal (Acq_dec) is zero). On the other hand, If Vth_2 is not crossed, the local code generator is delayed by a number of samples equivalent to the time interval $T_c/6$ (Tracking decision signal

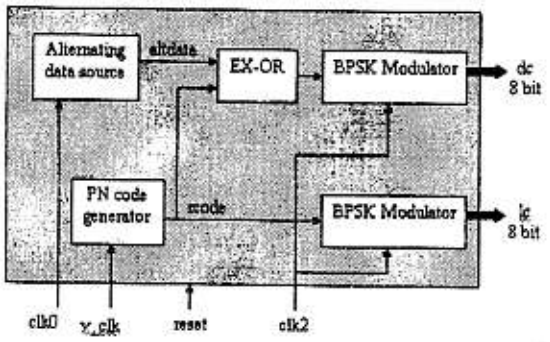

Fig.1 Architecture of local code generator

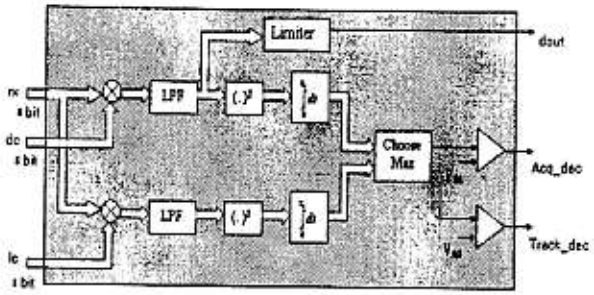

Fig.2 Traditional detector implementation

(Track_dec) is zero). The two delay options take their place using a variable clock signal (v_clk) for the local code generator. The limiter is used to produce the output data (dout, "either 0 or 1") at the same rate in that of transmitter by comparing the results of multiplications with a pre-setted threshold.

The FPGA cost of implementing this detector using Xilinx Virtex devices is the cost of implementing two 8 bit × 8 bit multipliers, two LPF filters, two squarers, two integrators along the correlation interval as well as the three comparators. Using Xilinx - virtex FPGA family, the cost and delay of implementing a logic expression of z input variables is given by [4]:

$$Cost=\begin{cases} 1 \ cells \ for \ z<4 \\ 2^{(z-4)} \ cells \ for \ z\geq 4 \end{cases} \quad ..(1)$$

$$Delay=\left\lceil \frac{z}{6} \right\rceil \ units \quad ..(2)$$

where [x] is the nearest integer greater than x. According to these equations, the cost of serial search synchronization scheme is discussed as follows : the cost of 8 bit × 8 bit multiplier depends on the algorithm used to implement the multiplier. If it is implemented using a set of 2 bit × 2 bit multipliers, the cost would be 120 cell with 4 delay units [5]. The cost and delay of LPF depends also on the algorithm used to compute the output, the number of filter taps and coefficients bit length. Using the algorithm in [6], the implementation of 21 tap, 8 bit length coefficients LPF requires 22 8bit adder/subtracter, 55 8 bit adders and 7 AND gates with a total cost of 1500 cell and 8 delay units. The squarer is an 8 bit × 8 bit multiplier so its implementation requires the same cost and delay of 8bit × 8bit multiplier. The integrator is an accumulator that adds 180 8bit samples during each correlation interval, and requires 38 cell and 8 delay units. The comparators (choose maximum and two threshold comparators) require the same cost of the proposed detector. The limiter is a one bit comparator (MSB) that requires 1 cell and 1 delay unit. Combining the cost of each element of the traditional detector, the total cost would be 3629 cell with 8 delay units.

III. FPGA Implementation of proposed serial search synchronization / detection scheme :

To minimize the cost and delay of FPGA implementation of the proposed synchronization detector in section II, a modified architecture is proposed for this detector as shown in Fig.3. This detector consists of three main blocks, ESB, MAXCORR and LIMITTER. The ESB (Extract Sign Bit) block isolates the sign bit from all the 8 bits symbols of input signals. The block MFSUM multiplies the received signal by the locally generated signals (only sign bits) and integrate the result The block LIMITTER takes its input directly from multiplier output and makes a decision on data value according to majority vote criteria on the samples over a fixed time interval equals transmitted data period. If the major samples is positive, the data is declared "1" otherwise declared "0". Fig.4 illustrates the architecture of the majority vote limiter.

The *significant contribution* in this proposed detector is the use of the fact that only sign bits of the received and locally generated signals are used to extract data which result in reducing all 8 bit mathematical operations to 1 bit operations and hence greatly reduce FPGA implementation cost. Fig.5 shows this fact. In Fig.5b, the signed symbol values of Fig.5a is replaced by the sign values only (1 for positive sign and 0 for negative sign). However, in both cases the data is extracted after multiplying the received and locally generated signals.

To be more accurate, the practical case is that the received signal is infected by an additive noise, therefore, some of positive signs may be converted to negative ones and vice versa. This problem is solved using the majority vote limiter. In fact, the

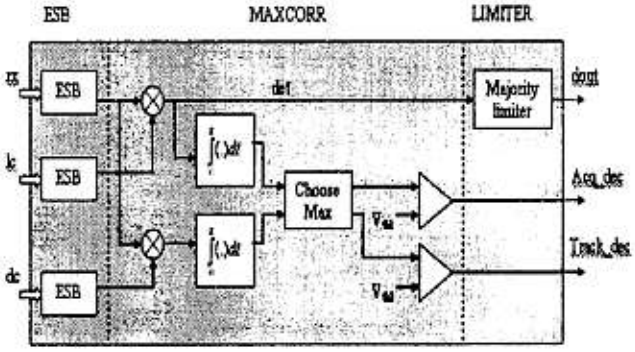

Fig.3 Architecture of the proposed detector

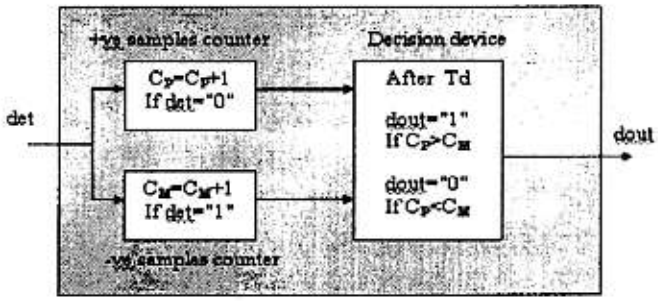

Fig.4 Architecture of majority limiter

capability of this proposed scheme to operate correctly depends on the signal – to - noise ratio as well as sampling rate value. Figures 6 and 7 show the probability of error of the proposed scheme (probability of incorrect estimation of data bits out from majority vote limiter) versus SNR with sampling frequency (F_s) as a parameter. In these two figures F_d is the frequency of data and F_o is the carrier frequency. This error probability is calculated using a huge statistical tests via MATLAB program. These two figures illustrate a surprise result that the cost reduction of our proposed detector offers very small penalty in error probability for SNR values greater than -2 dB. Hence for 5 dB SNR of our implemented system, the proposed detector is almost error free.

The cost of Xilnx FPGA implementation is discussed as follows :

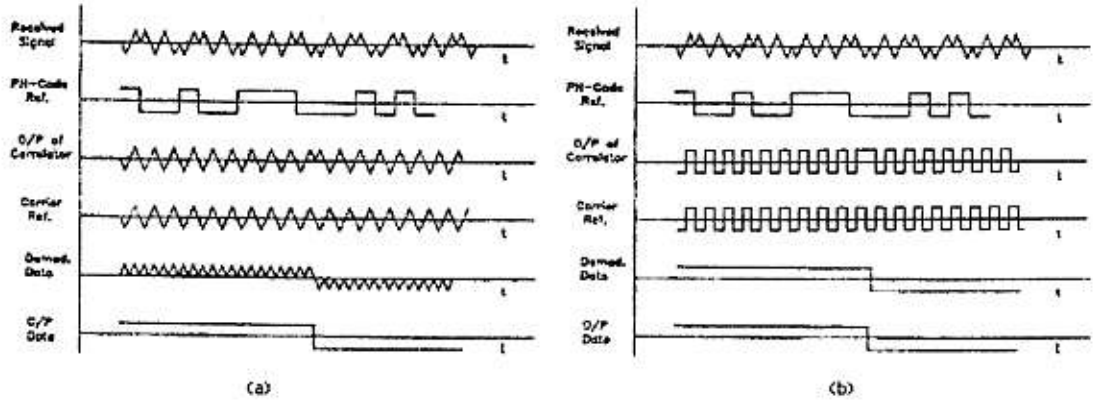

Fig.5 Waveforms at DS/SS detector
(a) Sinusoidal samples is represented by 8 bits.
(b) Sinusoidal samples is represented by sign bit only.

The ESB is just a buffer cost 1 cell with 1 delay unit in implementation. The two multipliers are each 1bit×1bit multiplier also costs 1 cell with 1 delay unit. The integrators are serial addition accumulators, their cost depends on the length of correlation interval. For our system, the correlation interval length is 30 chip i.e. there are 180 samples to be added which are equivalent to 8 bit adder with one serial input (since the binary representation of 180 needs 8 bit). If we use 2 bit adders to implement the 8 bit adder, this will require 8 cells and 4 delay units. The "choose maximum" block is an 8 bit comparator with 8 AND gates which require about 30 cells and 3 delay units in implementation if the comparison process in achieved in three stages, two stages of three bit comparators and one stage of two bit comparison. The two threshold comparators are also 8 bit comparators costs about 21 cell and 3 delay units. The cost of implementing the majority vote limiter depends on the number of samples within data duration which is 1800 for our system specifications. Designing for the worst case, the limiter is 11 bit adder (since the binary representation of 1800 needs 11 bit)

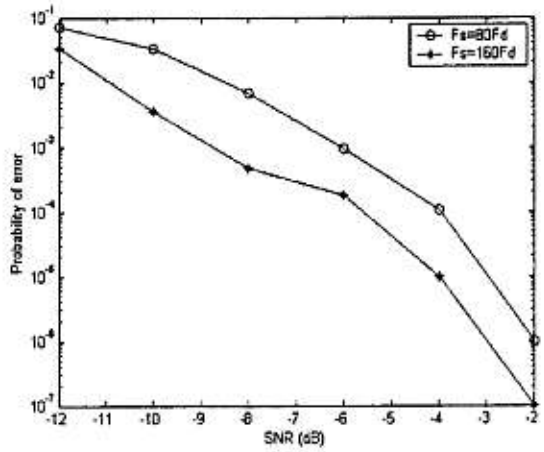

Fig.6 Probability of error versus SNR of the proposed detector $F_s=8F_o$.

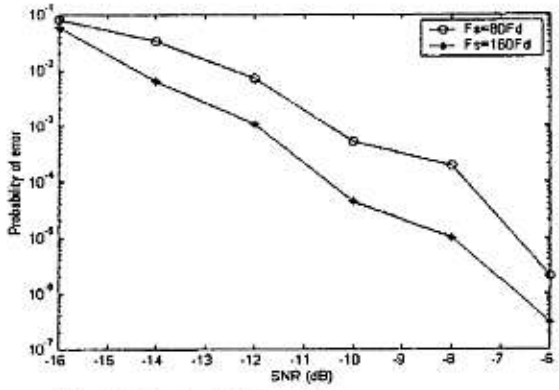

Fig.7 Probability of error versus SNR of the proposed detector $F_s=16F_o$.

and 1 bit comparator which requires 61 cell and 4 delay units. Adding the cost of each element in the proposed detector and considering the maximum delay among elements, the cost of implementing the proposed detector is 152 cell with 4 delay units.

Comparing the cost and delay of FPGA implementation of both traditional and proposed schemes, we conclude that using the proposed detector rather than the traditional one offers a cost reduction factor of 95.8% and delay reduction factor of 50%.

IV. Conclusions :

Xilinx-Virtex FPGA device is one of the efficient technologies that may be used to implement DS/SS synchronization subsystem. The design process could achieve good cost/delay optimization by rewriting the logic expression of each component in the system required to implement. A huge reduction in cost and delay may be obtained by extracting only the sign of DS/SS signal samples rather than the magnitude itself with acceptable error probability at middle values of signal-to-noise ratio.

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