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A Review of Modern and Recent Studies on the Low-Density Parity-Check Technology Approach

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Abstract- *Data theory coding is an excellent and well-known branch of study that has produced various crucial solutions to the insoluble challenges of safe data transfers. Last improvements in detecting error techniques have resulted in a significant increase in the use of low-density parity-check (LDPC) code to address critical concerns connected to secure data transfer. Until now, decent efforts have been performed on LDPC codes that target low complexity, high performance, and low bit error rate goals. The final aim of this review is to provide a recent literature understanding of modern improvements previously mentioned and in LDPC encoding and decoding (applicative and theoretical) techniques. A comparative scan of many remarkable LDPC decoding algorithms, 5G standard requirements, popular power management methods, and low-energy LDPC design studies is also shown. Lastly, conclusions are presented by outlining key study results, current concerns, and general thoughts on new research directions possibilities.*

Index Terms*— low-density parity-check encoder/decoder (LDPC), error correction codes (ECC), forward error correction codes (FEC), parity check matrix(PCM).*

I. INTRODUCTION

The wireless communication system can help us to deliver text messages through our phones or laptops to the desired destination throughout a medium or channel. But, these channels are not always safe or perfect for transfer. Messages can be corrupted, eroded, or even lost on their way to the final receiver; the reason for this noise could be the transmitter, the receiver, or the wireless communication channel itself. This problem is very common and can cause many issues, especially when sending sensitive data such as banking information. That is why we need robust error correction codes (ECC). Algebraic and probabilistic are the two basic types of ECCs. The probabilistic part can achieve comparatively high throughput and maintain a reasonable level of design complication compared to the algebraic. The basic benefit of the first is the powerful correcting ability, that grants a fewer bit error rate (BER) [1].

Because we may fix bits without retransmission, ECC is also known as forwarding error correction (FEC). A digital source of information gives input data to the encoder inside of communication system that uses (FEC) coding, extra bits (or parity) are added by the encoder, resulting in a larger sequence of code bits known as a code word, that will be broadcasted to the recipient, where the actual data stream can be recovered using decoder in it. FEC increases data dependability and performance by inserting a predefined structure together into a data sequence before sending or storing [2]. LDPC is an error-correcting technique utilized in unsafe communication channels for reducing data loss. Which could

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be decreased to minimal with LDPC, allowing data transmission percentage to be as near as possible to Shannon's limit.

In 1960, Robert Gallager [4] created LDPC in his Ph.D. dissertation at MIT. Three years later, it was released by MIT Press. For nearly 30 years, LDPC was ignored due to the computational effort required to create the encoder and decoder for them and Reed-Solomon codes development. During that time, the only work on LDPC was done in 1981 by R. Michael Tanner, when he extended them and provided graph depiction for them, which became known as the Tanner graph. With the efforts of Mackay and Luby, LDPC was recreated[5,6]. By comparing every type of ECC, it has been noticed that they are different in correcting performance, computing approaches, and implementation complexity [2]. However, LDPC codes outperform Bose-Chaudhuri-Hocquenghem (BCH) and Reed-Solomon (RS) techniques for extended codeword lengths[5]. They have also been shown to provide appropriate parallelism and robustness[6] and can outperform Hamming codes, Reed-Solomon codes, and Reed-Muller codes, according to their high BER [7]. Additionally, LDPC has the following features compared to turbo codes: better performance when the block length is significant, high flexibility, easy demonstration and resulting theoretical verification, lesser complexity in decoding, a parallel possibility that makes hardware implementation easier, and high throughput that offers fast decoding [8], [9].

Whereas the design of particular processing elements is slightly streat forward, the structure of the entire LDPC decoder is affected by many relationships with several design limits, such as processing throughput, processing latency, hardware required resources, abilities of error correction, processing energy, bandwidth efficiency, and flexibility, code rate, and length, all was taken into account when designing LDPC codes for the 5G standard. Various system elements, such as the architecture, method, usage, and the decoding cycle number, also affect the characteristics of the design [10],[9]. On the other hand, Cycles (a series of related nodes that starts and finish at the same node), tended to decrease LDPC code decoding efficiency. As a result, short cycles must be prevented while developing LDPC codes[11], [12].

Despite that, standards use LDPC-codes extensively such as Wireless LAN (IEEE 802.11n), mobile WiMAX (IEEE 802.16e), digital video broadcasting (DVB-S2), 10 Gigabit Ethernet (10GBaseT), Wi-Fi, ATSC 3.0 and 5G, and several upcoming standards are expected to include it [4], [7], [10], [13], [14].

This paper's structure is as follows: Section II introduces LDPC types and structures, as well as their benefits, and delves into its characteristics. Section III presents and examines possible designs as well as comparisons to earlier studies. Section IV depicts the basic design and types of LDPC encoder. Section V gives an overview of the basic design and types of LDPC decoders, as well as their benefits. Section VI, along with the conclusion, and a collection of open issues and concerns surrounding LDPC design.

II. TYPES AND REPRESENTATION OF LDPC

LDPC is a set of direct codes with a small equality check medium. It could be represented in two manners: either in parity check matrix H or using tanner graph, which is simply bipartite graphs, used to express LDPC in a graph representation. Two types of nodes in the Tanner graph: variable nodes, which define a single column in the parity-check matrix, as well as check nodes, which define a single row in the parity-check matrix [11]. The sparsity of the H matrix means that there is less number of 1's than zeros, which will

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help LDPC codes expand in the smallest amount of space. The minimum distance of LDPC codes climbs linearly as the codeword length increases, and each coded Bit has the same amount of parity check equations. However, there are two types of LDPC codes as shown in *Fig. 1*. binary and non-binary. Binary LDPC has an advantage in correcting errors and the capacity of channels for large block lengths. Low word lengths perform worse cause of the small cycles in the parity matrix (Binary LDPC are separated into irregular and regular LDPC, it will be regular if the column and row weights are consistent. Else the code is irregular. Gallager's LDPC code is regularly built by randomly selecting the positions of 1's with fixed integers in each row and column [15],[14].

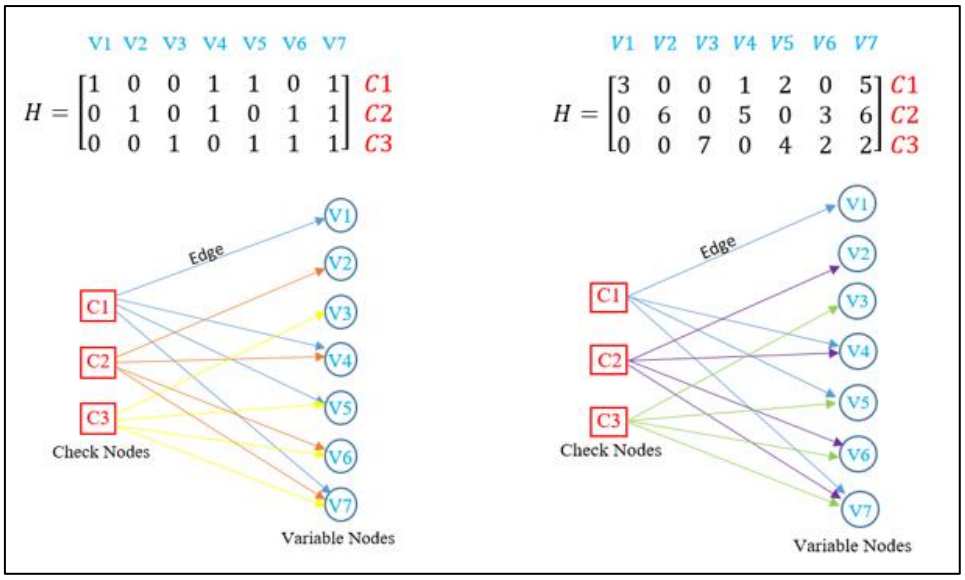

FIG. 1. SHOWS REPRESENTATION OF LDPC IN MATRIX FORM AND GRAPHICAL FORM NAMED AS TANNER GRAPH, THE ROWS REPRESENT THE CHECK NODES (C1, C2, C3) ALSO EQUALS THE NUMBER OF EQUATIONS NEEDED, COLUMNS REPRESENT THE VARIABLE NODES (V1…V7), THE CONNECTION BETWEEN BOTH ENDS CALLED (EDGE). THE FIGURE ALSO SHOWS THE DIFFERENCE BETWEEN THE BINARY (LEFT-HAND) AND THE NON-BINARY LDPC MATRIX (RIGHT-HAND SIDE).

There is a lack of an ordered framework of published studies concerning non-binary LDPC and their applications, such as Space Communications, Optical Communications, Data Storage, and Power-line Communication, capable of obtaining superior BER performance for modest code lengths. However, this comes with the cost of complexity[1]. Nowadays, The data channel and control channel of the 5G mobile communication technology use polar code and block code (BC) LDPC. Despite their outstanding effectiveness, these methods have apparent drawbacks. Low decoding progress, high complexity, and significant decoding delay are some of the disadvantages of the BC-LDPC. Meanwhile, it performs poorly in shortcode length and code rate. According to the serial decoding computation, polar code has an abnormally high decoding latency for lengthy code lengths. More reliability, reduced delay, and larger throughput would be needed to face the actual large rate data transmission requirements of the future 6G Concerningrespect to low error level, shorter decoding duration, and low decoding complication, the convolutional code (CC) LDPC that was proposed by M. Lentmaier, and A. Sridharan that offers tremendous promise [7],[8],[16].

Another two samples of LDPC codes are QC-LDPC and MET-LDPC. The last has an advantage over ordinary irregular LDPC codes due to the multi-edge type structure of their parity-check matrices. QC-LDPC is recognized as appropriate for implementation in

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hardware. The consistency in their PCMs allows them to perform decoding in parallel with a shift register and get high memory effectiveness [9]. Existing error-correcting approaches based on LDPC were less suitable for sophisticated service-oriented challenges requiring more than one solution. This is a prevalent case in 5G technology, where error-free facilitation necessitates adaptability and flexibility to accommodate a large area of lengths and code rates. In addition, the decoder design has to provide appropriate parallelism and suitability for enabling multi-mode standards capable of achieving large peak throughput in hardware [17]. It has been demonstrated that LDPC decoders can generate several to hundreds of Mbit/s. Moreover, because of a static instruction set of GPU and CPU foundation architectures, worries taken by LDPC developers can differ significantly from those taken when creating hardware custom-made for LDPC decoders[18]. The need to tackle topical difficulties of the applied and theoretical layout of LDPC in communication links leads to a critical technical and scientific problem: formalizing the mathematical representations for constructing trustable codes within LDPC. The need for mistake repair must be investigated. To offer the set indications of noise and immunity in data transmission networks, it is required to analyze LDPC at various rates and numbers of decoding iterations[19].

III. RELATED WORKS

The development of LDPC encoding and decoding methods has inspired the creation of numerous articles discussing the implementation of these codes. On FPGA devices, in terms of their various features, such as algorithm type used. Type of LDPC used and purpose of implementation. Whether to improve performance, reduce complexity, increase throughput, and so on, such as the following [1]–[3], [11], [15], [17]–[21] conducted a comprehensive survey on LDPC code encoding and decoding techniques (in both academic and industry).

[22], [23] propose a simplified LDPC decoding algorithm to lower implementation complexity, and implemented it on the FPSimilarlylar manner, [24] compares the performance and implementation complexity of LDPC decoders. [5], [25]offer a probabilistic algorithm novel low-complexity, high- productivity Bit Flipping (BF) LDPC decoder over Binary Symmetric Channel (BSC). Including a hardware implementation design for PPBF, on the other hand [26], compares the performance of the Probabilistic Gallager B (PGaB), complex decision message passing LDPC decoder, to the soft decision MinSum (MS) decoder and the implementation them Xilinx Virtex6 Field Programmable Gate Array (FPGA).

[27], [28] discuss and contribute the implementation details requirements of the new 5G NR channel coding platform. Similarly, [9], [13], [29] offer a 5G NR LDPC decoder, and some report a practical hardware architecture and implementation results for 5G-NR LDPC decoder utilizing the FPGA Xilinx Ultra scale XCKU060. [14],[30],[31] offer a high-performance architecture of LDPC decoder on reconfigurable FPGA hardware, Utilizing different algorithms such as Min Sum and bit flipping algorithm. When it comes to power and energy management, could be observed that [32]–[35] suggest power management strategies based on performance needs and resource availability using the DVFS technique. Furthermore, [36], and [37] examine designs for LDPC decoders that can operate at low voltage and power conception.

In digital communication networks, turbo codes are commonly employed, [38]–[40] studied the layout and synthesis of turbo code and enhancement of it utilizing Altera

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Cyclone II FPGA board and MATLAB software. Equally [41],[42] present the design and implementation for turbo and LDPC decoding needs for high-throughput applications. Nevertheless, [43]–[46] presented a framework and improved error rate performance and compared FFT and DCT-based Orthogonal Frequency Division Multiplexing (OFDM) systems. while [47] discusses the performance of a spatial multiplexed wireless OFDM transmission method with LDPC based on a Sniffer Mobile Robot (SNFRbot). Furthermore, [16],[48],[49] explore and review and provide Techniques for the encoding and decoding of channel codes, such as CC-LDPC, Semi-LDPC-CC, BC-LDPC, and polar code. Others investigate LDPC in varied fields and new designs to improve them, such as in [6], Using the HLS-based technique, proposed a general SystemC behavioral model that can be used to construct hardware efficient LDPC decoders with Xilinx Vivado HLS. This principle is focused on the vectorization paradigm of single instruction multiple data (SIMD).

Nevertheless, [7] investigated the error correction in WSN using short-length LDPC. They examine the power consumption, implementation, resource requirements, and designs of LDPC decoders to see their appropriateness for use in WSN sensor nodes. [12] observed that the implementation in the hardware of variable node and check node in HDL code is quite time-consuming and complex. As a result, they suggested a concept based on Min Sum LDPC decoder. This method also aids in shortening the time required to evaluate and test the variable node and check node designs. Besides [50], a generalized algorithmic method of constructing node processing units (NPUs) supports flexibility in run-time while keeping small hardware alternative demands and a large operating frequency and support for flexibility in inter or intra-standard LDPC at operating time.

Reference [53] offered a novel method for LDPC decoders which is high-throughput hardware design and cost-effective. with the same purpose. Moreover, [51] observed that protograph and ARA-based LDPC codes could achieve error efficiency comparable to sample elevated codes and benefit from many design advantages due to their structure. The suggested architecture by [52] is about the structure of quasi-cyclic (QC-LDPC) codes, whose performance is compared to LDPC for intermediate and short block sizes.[53], establish novel techniques for generating regular and systematic Low-Density Parity-Check Matrices (LDPCM), influenced by geometric patterns and the Sarrus method. Moreover, [54] gives their vision of 6G and explains utilization cases and needs for intelligent 6G and multi-terabyte per second (Tb/s). [55],offer a large data-rate LDPC decoder appropriate to use in 802.11n/ac (WiFi) standard. They present more accurate log sum-product method approximations that work for lower signal-to-noise ratio requirements.

Focusing on the LDPC error floor, to improve coding gain arrives at the expense of increasing complication or bit rate, and it is demonstrated were [56] demonstrated that a combination system based on LDPC as an internal code and the Bose, Chaudhuri, and Hocquenghem codes (BCH) as an exterior may lower error limit.The effect of LDPC upon system performance across Additive White Gaussian Noise (AWGN) with Binary Phase Shift Keying (BPSK) and some random fading (Raleigh and Rician) channels has been examined by [57]. The results demonstrate that LDPC is capable of enhancing transceiver systems for many channel types. Convolutional code limits performance supporting low-bandwidth transmission across Rayleigh fading channels and AWGN [58].

In a different manner [59], create and apply an empirical path loss model (Samir Model) for WiMAX network planning. To keep intruders from getting the transmitted data, [60] published an enhanced Method for Information Hiding using Hybrid Encryption and Steganography.

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[61], concentrate on the essential crucial parameters needed to design and analyze digital communication systems with lower signal-to-noise power ratio (LSNR) conditions. In an applicative manner, the research results in [62] reveal that developing and understanding the implementation of software-defined radio (SDR) using programmable logic tools is simple. Integrated MatlabTM blocks, Matlab/SimulinkTM, Cyclone II and training platform are used for implementation. [63], proposes a new algorithm for combining three CRC circuits, which test the integrity of transmitted data, into one to reduce the total size of the transceiver utilizing Altera FPGA.

A new field [64] proposed two approaches employing the Viterbi algorithm to identify crimes using crime databases from Iraq and India. [65], provide multidisciplinary software modeling and analysis of a 3210 Gb/s Wavelength Division Multiplexing all-optical bidirectional hybrid communication system for exterior usage. By optimizing the transmitter and receiver design parameters, the efficiency of a multiwavelength free-space optical (MFSO) communication system was improved [66].

Databases of the previously mentioned studies are declared in Tables I and II. We attempted to limit special designs of LDPC in Table III to examine the benefits and drawbacks of each.

TABLE I. STUDIES THAT HAVE BEEN REVIEWED IN THIS PAPE BELONG TO THE IEEE DATABASE

REFERENCE NO.	JOURNAL	YEAR
[1]	IEEE explore	2021
[5]	IEEE Transactions	2018
[8]	IEEE Communications Magazine	2018
[9]	IEEE Transactions on Broadcasting	2019
[10]	IEEE Communications Surveys and Tutorials	2016
[36]	IEEE Journal of Solid-State Circuits	2008
[18]	IEEE Access	2016
[21]	IEEE Communications Surveys and Tutorials	2011
[20]	IEEE 25th International Symposium on On-Line Testing and Robust System Design, IOLTS 2019	2019
[22]	IEEE Transactions	2008
[23]	Design, Automation and Test in Europe, DATE- IEEE Explore	2007
[27]	IEEE Access	2021
[29]	IEEE International Symposium on Circuits and Systems	2019
[30]	IEEE Communications Letters	2018
[32]	IEEE Transactions on Multi-Scale Computing Systems	2018
[35]	IEEE Access	2019
[37]	IEEE Transactions on Very Large Scale Integration (VLSI) Systems	2010
[42]	IEEE International Symposium on Spread Spectrum Techniques and Applications	2008
[48]	IEEE Symposium on Computers and Communications	2017
[50]	IEEE Transactions on Circuits and Systems II: Express Briefs	2018
[67]	IEEE Transactions On Very Large Scale Integration (VLSI) Systems	2018
[68]	Midwest Symposium on Circuits and Systems-IEEE	2017
[52]	IEEE International Symposium on Circuits and Systems	2007
[54]	IEEE Vehicular Technology Magazine	2019
[55]	IEEE Transactions on Very Large Scale Integration (VLSI) Systems	2018

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TABLE II. STUDIES THAT HAS BEEN REVIEWED IN THIS PAPER THAT BELONG TO THE SPRINGER DATABASE

REFERENCE NO.	JOURNAL	YEAR
[3]	Springer Series in Advanced Microelectronics	1962
[6]	Journal of Signal Processing Systems-springer	2020
[17]	Archives of Computational Methods in Engineering- springer	2021
[41]	Journal of Signal Processing Systems-springer	2011
[46]	Optical and Quantum Electronics- springer	2021
[47]	Institute for Computer Science, Social-Informatics and Telecommunications Engineering- springer	2009
[65]	Optical and Quantum Electronics- springer	2021
[66]	Optical and Quantum Electronics- springer	2020

TABLE III.THE ADVANTAGE AND DISADVANTAGES OF LDPC STUDIES

REFERENCE NO.	YEAR	ADVANTAGE	DISADVANTAGE
[4]	2014	The suggested algorithm has low complexity and outstanding performance compared to the bit-flipping technique.	this method does not employ the iterations approach, which enables the detection of faults introduced by the transmission channel to be done fast and efficiently.
[6]	2020	LDPC decoders using high-level synthesis(HLS) are shown.	Furthermore, it does not detail the design of an entire accelerator, having integration and analysis with a whole processing platform based on a physical layer.
[7]	2014	The results reported are from a real-world FPGA design; therefore, real-world hardware functionalities and performance have been evaluated and checked, unlike others.	The test results reveal that LDPC is suitable for WSN usage. On the other hand, LDPC codes need complicated decoders with powerful hardware and power consumption.
[23]	2007	The synthesis findings related to WiMAX and single-standard LDPC decoders developed usage has been presented, and both decoders can reach a significantly high throughput-to-area ratio (TAR).	When the routing area is considered when analyzing the outcomes of the decoders presented, the TAR (normalized TAR) values of decoders are substantially influenced.
[25]	2017	The flipping process can be carried out on a probabilistic basis. The error-correcting efficiency of the Probabilistic Parallel Bit Flipping (PPBF) decoder is comparable to that of the Gradient Descent Bit Flipping (GDBF) decoder.	However, there is still a significant performance difference between the soft-decision and PGDBF algorithms.
[27]	2021	Adapted min-sum (AMS) decoding was introduced to lower the error risk of degree-1 VNs, in which independent methods handle the core and extension checks.	Compared to belief propagation (BP) decoding, AMS performance is still weak.
[37]	2010	The bypassing strategy has been presented that efficiently minimizes memory access and energy usage.	However, because this code-specific architecture has no broad applicability, it may have difficulty adapting to other platforms.
[42]	2008	The system on chip (MPSoC) design of a multiprocessor is detailed for Turbo and LDPC decoding.	The Throughput of LDPC in the suggested design is low compared to other similar works.

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[50]	2018	As can be observed, the suggested dual-tree architecture requires fewer hardware resources and has a greater maximum running frequency than the other general-purpose alternatives.	To be able to accommodate over than single coding rate. A routing network or a method is utilized for combining processing units for decoding to assist more than one code length or code rate to larger optimize its system power. Nonetheless, complicated linkage degrades time, which will lead a concurrent digital system to fail.
[52]	2007	The suggested decoder improves throughput, flexibility, area, and power.	It may demand a lot of memory requirements.
[53]	2020	We can observe that for small-length matrices, the effectiveness of the suggested matrices meets or outperforms the current approaches for constructing parity check matrices.	Even though the approach can generate LDPC codes of any length, it achieves exponential complexity and can only build regular LDPC codes. Also, no power calculations are mentioned.
[55]	2018	The suggested decoder in terms of adjusted throughput rate beat all Wi-Fi and multi-standard decoders.	Generally, high frequency requires higher power consumption.

IV. LDPC ENCODER

The LDPC code encoding process consists of two steps: Create a sparse parity-check matrix and use it to produce codewords c of size n :
$c = (a0.a1 \dots \dots a_{(m-1)}.q0.q1 \dots \dots q_{(n-m-1)})$ by encoding a Bitstream block
$c = \left(a0.a1 \dots \dots ia_{(m-1)}\right)$ of size k, so that $H * c^T = 0$, where H is the PCM, and $n - m$ are parity bits [31] [2].

The first encoding type was proposed by Gallager in [3], and developments continued until reaching the second type of encoding presented in [69], where a flexible and moderately hardware efficient LDPC encoder was built. The encoder of this type can be constructed with some level of parallelism.

For the family quasi-cyclic LDPC codes the author in [70] provides LDPC encoding approaches and architectures that are efficient and feasible for a particular type of code. These are LDPC for the irregular partitioned permutation. This study extends that primary method by utilizing other structural aspects to enable a more straightforward and faster encoding procedure in software and hardware.

V. LDPC DECODER

We may increase error-correcting capabilities, like employing a robust LDPC code or several decoding rounds. An increase in the number of iterations increases complexity and, as a result, decreases processing energy efficiency while increasing transmission energy efficiency. Also, while designing an LDPC decoder, the overall energy dissipation should be addressed holistically. Because the decoder must simultaneously analyze every conceivable message word (such algorithms are frequently referred to as iterative), decoding an LDPC codeword is substantially more complicated than encoding. It is essential to execute an LDPC decoder architecture to sufficiently define it.

The easiest method is employing a Field-Programmable Gate Array (FPGA) chip, which allows for quick parallel logic processing and prototyping [10],[13]. Many characteristics influence the difficulty and performance of an LDPC decoder, including block length, coding rate, processing node complexity, interconnection complexity, number

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of repetitions, and parallelism level. As a result, there is a sense of balance between the decoder's performance and the difficulty of decoding[15].

LDPC may be decoded efficiently by using soft-information message-passing decoders such as Sum-Product (SP) and Min Sum (MS), as well as hard-decision decoders for example Gallager-A, and B, Bit Flipping (BF), as shown in *Fig. 2.* Due to their low-complexity design, fast decoding throughput, and ongoing development in error correction, hard choice decoders have lately gained a lot of interest, nearing or overcoming soft-decision decoders.

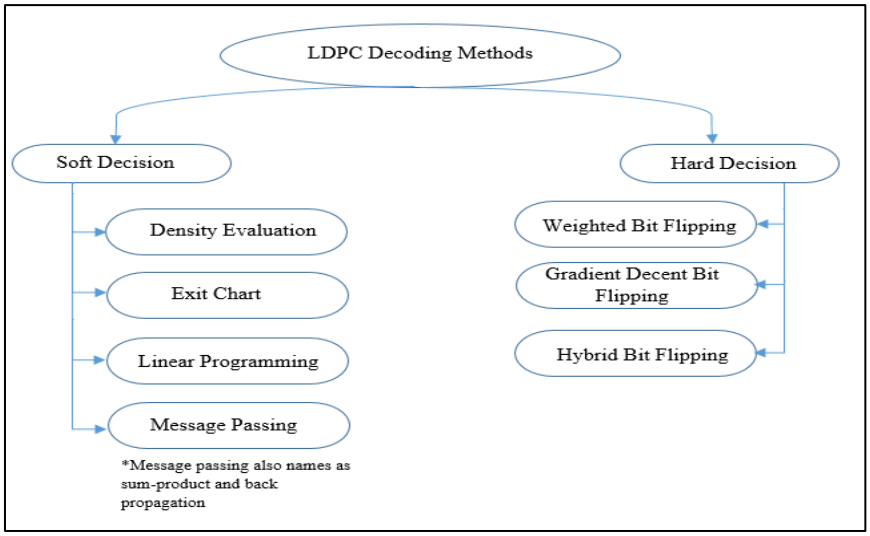

FIG. 2. TYPES OF LDPC DECODING ALGORITHMS [17].

The LDPC decoding is a repeated procedure where messages are transmitted sequentially between Variable Nodes (VNs) and Check Nodes (CNs) computational units, along tanner graph edges, as shown in *Fig. 1*. The low complexity of hard choice decoders is because just 1-bit messages are sent from VNs to CNs, simplifying linked networks. [25],[29].

Min-sum decoding is an iterative message-passing decoding popular in LDPC decoders due to its high BER performance and straightforwardness. Every decoding round involves updating and transmitting extrinsic signals within nearby variables and checking points[36]. The min-sum decoding technique, a subset of the sum-product algorithm, minimizes computing complexity while making the decoder numerically reliable[7]. *Fig. 3* demonstrates the LDPC encoder and decoder job in the communication channel.

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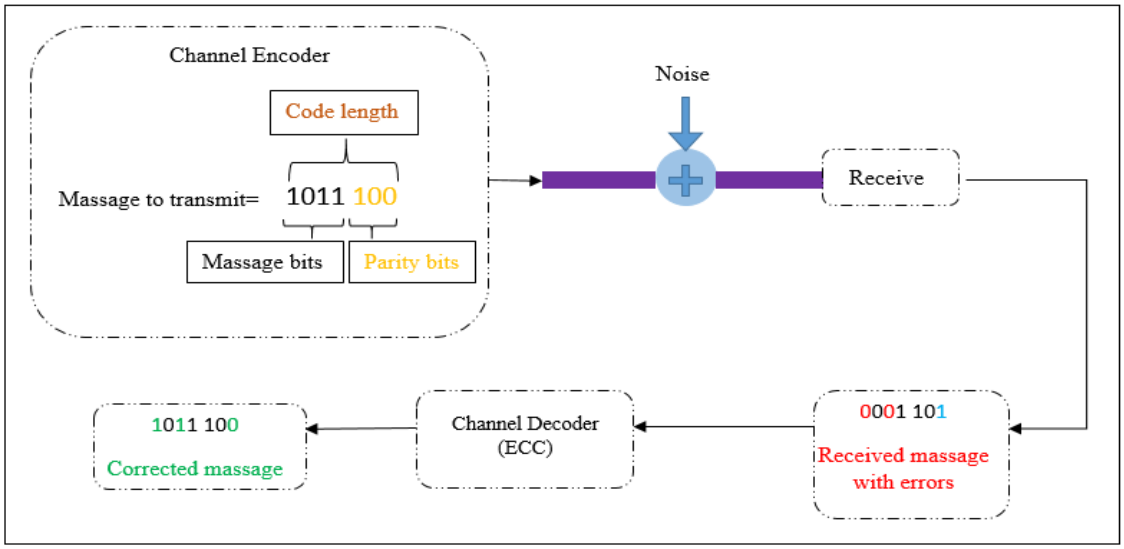

FIG. 3. AN ECC SYSTEM IS SHOWN. THE ORIGINAL MESSAGE BITS ARE REPRESENTED BY $\boldsymbol{K}$ AND CODE LENGTH (WHICH IS THE ORIGINAL MESSAGE BITS WITH THE PARITY BITS) COULD BE CHARACTERIZED AS $\boldsymbol{N}$, AND PARITY BITS COULD BE REPRESENTED BY $\boldsymbol{N-K}$; AS A RESULT, THE CODE RATE OF THE MASSAGE WILL BE THE RATIO BETWEEN THE ORIGINAL MESSAGE AND CODE LENGTH $\boldsymbol{R}=\frac{K}{N}$ [4]. THIS DATA WILL BE SENT VIA THE CHANNEL AND EXPOSED TO NOISE. SOME OF THE BITS WILL BE CORRUPTED OR ERODED WHEN THEY GET TO THE RECEIVER. THE ECC SYSTEM CORRECTS MISTAKES AND SERVES AS THE FOUNDATION OF DEPENDABLE DATA TRANSFER SYSTEMS.

The sum-product algorithm (SPA) was the first method to decode LDPC. The SPA transforms channel input into a log-likelihood ratio (LLR). Where LLRs are known as $L(c)=\log(\frac{P_{(c=0)}}{P_{(c=1)}})$ where c is a bit of the frame in the decoding process[6]. The LLR is sent to the variable nodes, which are kept up to date by the variable node process defined in equation (1).

$$V_i = LLRn + \sum_{j\neq 1} C_j \dots\dots\dots (1)$$

Where $n = 1.2 \dots etc$ variable nodes number and $i.j = 1.2 \dots etc$ variable node degree. The action of a check node is given by equation (2).

$$C_k = 2\tanh^{-1}\left(\prod_{k\neq l}\tanh\frac{V_l}{2}\right)\dots\dots\dots (2)$$

Where $l.k = 1.2 \dots etc$ check node degree. In SPA, various nonlinear behaviors are required in check nodes, and large-accuracy external messages are transmitted between the nodes. This indicates a large level of computational complexity. On the other hand, SPA achieves excellent decoding performance [12]. SPA necessitates exponential functions; it is unsuitable for effective hardware implementation. To simplify the decoding technique, the author in [6] introduced and studied the developed history and equations of the Min-Sum algorithm and also presented error correction performance and computing complexity trade-off.

Unlike, the min-sum algorithm in [7], a subset of the sum-product algorithm, minimizes computing complexity while also making the decoder numerically stable. A variable node in the min-sum decoding executes the process shown in equation (3) and then results are delivered to check nodes.

$$L_{cv} = \sum_{m\in M(v)\backslash c} R_{mv} + I_v \dots\dots\dots (3)$$

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Where I_v: variable node input v, recognized as (LLR).
L_{cv}: variable node output v traveling to check node c.
$M(v)\backslash c$: a group of check nodes linked to variable node v, without the check node c.
R_{mv}: check nodes output traveling to variable node v.

A check node gets messages along with the tanner graph from the variable nodes and performs the operation in (4):

$$R_{cv} = \prod_{n\in N(c)\backslash v} sign(L_{cv}) \times \min_{n\in N(c)\backslash v} |L_{cv}| \dots\dots\dots (4)$$

R_{cv}: check node output c moving to variable node v.

All check nodes examine the signal of the information getting out from variable nodes to see if the parity constraint is met. Messages then transmitted back to variable nodes till parity state are fulfilled for each check node, at a point which the decoder terminates the operation. The min-sum decoding takes advantage of soft decisions. Although, a hard decision has been made regarding the late LLR (I_v). If it is passive, the output bit is a 1; else, it is a 0 [7].

Through the literature, to highlight two forms of layered decoding schemes: vertically stacked decoding as well as horizontally layered decoding. In the last, a one or a fixed number of check nodes (known as layers) are updated at first. All groubs of nearby variable nodes is then refreshed, as well as the decoding process will continue layer at a time. Within vertically layered decoding, an individual or a subset of variable nodes (layer of variable nodes) are updated first. The entire set of surrounding check nodes is then refreshed. Horizontally layered decoding is preferred for practical applications since the serialized check node processor looks simpler for implementation in VLSI. Layered decoders are typically found within LDPC due to their fast computation and regular construction design [37].

Decoder LDPC architecture has three types: entirely parallel architecture, halfway parallel architecture, and serialized architecture. Within a completely identical architecture, the processor of check nodes is required for each one, which will typically produce high hardware costs and convoluted connectivity, making the architecture lesser adaptable. The serial design is too sluggish among most applications since it utilizes only one check node processor for dividing the computations of all the check nodes. For half parallel architectures, many processing units have been used, providing for a reasonable compromise among hardware cost and performance, and are often used in practical implementation. The layered decoding algorithm is the second name for serialized message passing algorithm, with the partially parallel architecture, and its variants are utilized to accomplish faster convergence, i.e. for reducing the number of decoding cycle [37].

VI. CONCLUSIONS

This study thoroughly examines the fundamental principles of LDPC and its encoding and decoding schemes and performance measurement, comparisons, and applications. The general analysis of existing decoding design techniques and their advantages and disadvantages is done succinctly. According to the analyzed articles, computational cost, low energy, and high performance demand additional research and experimental testing. Numerous notable scholars have suggested substantial decoding algorithms based on LDPC codes to address these challenges.

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Most of these existing approaches have demonstrated their success in improving decoding performance while requiring minimum complexity; some of the traditional design strategies could be combined with various methods to add more efficiency and effectiveness. Despite it being a strong candidate, many concerns related to the design such as power and complexity can be addressed through more research and testing, making LDPC codes applicable to a wide variety of essential telecommunication services and devices.

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