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High Rate Data Processing System of 6x6 MIMO_OFDM Using FPGA Technique with Spatial Algorithm

Abstract*—OFDM has high spectral Performance and pliability in multipath channel effects while MIMO use another strategy for saving power of transmitter by using multi in multi out antennas to make throughput processing in high efficiency. The transceiver MIMO OFDM implemented on an FPGA typeSpartan3 XC3S200 with proper algorithm, Invoke method and QPSK modulation. The project prospective to improve the transceiver operations in terms of data transmission in high speed and saving power for wireless communication system take in consideration the cost of implementation hardware. In the result registered throughput data rate 425 Mbps using spatial algorithm (ICA with SD algorithm) with another advantage reduction in PAR by 6db and BER less than 10-7).The total architecture using 61% slice registers, LUT's of 55% and memory about 67% on board of Spartan-3 XC3S200.*

Keywords- *MIMO, OFDM, FPGA, PAR (Peak to Average power Ratio), ICA (Independent component analysis algorithm) with SD (sphere decoding algorithm).*

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1. Introduction

Limited spectrum frequency and limited power is the main challenges confrontation in modern wireless communications that satisfy increasing speed of data transmission [1]. Multimedia services, internet, cellular mobile and other wireless communications systems required large capacity to realize request huge amount of data rates. This guide to find way to increase the capacity in order to increase throughput data rate of communication system, MIMO-OFDM is one of the most way using for this requirements [2,3]. OFDM overture spectral of high efficiency and pliability effects for the multipath channel. The technique of OFDM make communication channel divides into a numbers where the frequency bands of it are equally spaced [4,5]. Section II describe the transceiver OFDM details with PAR reduction using spatial algorithm (ICA with SD algorithm). Section III deals with system design methodology, section IV describe model Simulink, its subsystem transceiver module. Section V deals with simulation results. The data transmitted in each band frequency is carried by a subcarrier. The design flow diagram of the synthesizers is used in Xilinx Integrated Software Environment (ISE).The hardware block simulation used Modalism to verify it by using Vectors test produced by benches test HDL or generator system. Finally the FPGA board programmed by the bit streams generated, ISE used to report the blocks performance and synthesis results.

2. OFDM Transceiver

The OFDM transceiver shown in Figure 1, the input bits arranged into blocks of size log2H where H is the size of constellation signal. The designers system is usually response to chosen the scheme modulation or depending on the systems of the wireless communication requirements [6,7].
The mapped processing into symbol modulated covered all the bits block denoted as Z[H],using the constellation signal scheme modulation. The conversion from serial to Parallel order involve for the output signal before applied to IFFT then converted again to serial order. The mathematical formulation for the yth signal in MIMO-OFDM system is:

$$F_y(t) = S_y e^{j\emptyset y} Z_y(t) \quad (1)$$

Where S_y and ϕy are the phase carrier and signal amplitude while $Z_y(t)$ represent by:

$$Z_y(t) = \sum_{k=0}^{C-1} Z_y(k)\, u(t - kS - \tau_y) \quad (2)$$

where k is the block index and C is the length block depending on the number of subcarrier, $Z_y(k)$ is the vector blocks of signals received per

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subcarrier y for y=0,1,….,(C -1),t is the time step, kS is the one cyclic block time,τ_y is redundant time prefix cyclic and u is the vect-or function block time. The data transmission use IFFT and FFT for the transceiver system, where the data split into blocks which are discrete by interval guard and the guard bit used to remove interference inter block [8,9].

$$M_r(b) = \sum_{\rho=0}^{v-1} n(\rho) l_r(b-1) \quad (3)$$

Where *Mr(b)* is the transmitted antenna r signal encoded, the encoder convolution with the actual amount of impulse response $n(\rho)$ used from distribution identical independent and variance unit to encoded data $lr(b)$ and the length v to get the transmitted antenna(r)encoded signal.
The signal encoded then carried out in blocks $Mr(k) = [mr(KC), mr(Kc1, \ldots., mr(kC + C - 1)]^T$, the prefix cyclic used for converted channel selective frequency into channel fading flat and that is happened in all subcarrier [10]. After the signal transfer into blocks, the complete received signal expressed by:

$$F(y) = H(y)M(y) + n(y) \quad (4)$$

Where *F(y)=[F1(kC +y), F2(kC +y),…..,FCf =(kC +y)]*^{T}and *Fi(.)* is signal from antenna receive i can build by take in consideration C_T antenna transmitter and Cr antenna receiver.
Where

$$H(y) = \begin{pmatrix} \text{H11(y)} & \text{H12(y)} \ldots\ldots\ldots & \text{H1Ct(y)} \\ \text{H21(y)} & \text{H22(y)} \ldots\ldots\ldots & \text{H2Ct(y)} \\ \vdots & \vdots & \vdots \\ \text{HCr1(y)} & \text{HCr2(y)} \ldots\ldots\ldots & \text{HCrCt(y)} \end{pmatrix}$$

and *Hcr(y)* represent the yth channel coefficient DFT between antenna transmitter Ct and antenna receiver *Cr.* The transmitted signal per subcarrier y is given by

$$M(y) = [M1(KC + y), M2(KC + y), \ldots., MCt(KC + y)]^T$$

Where *Mt(.)* is transmitted signal by transmit antenna Ct and $n(y)$is vector of additive white Gaussian noise (AWGN) with variance $C0$ and mean zero coefficient [11].

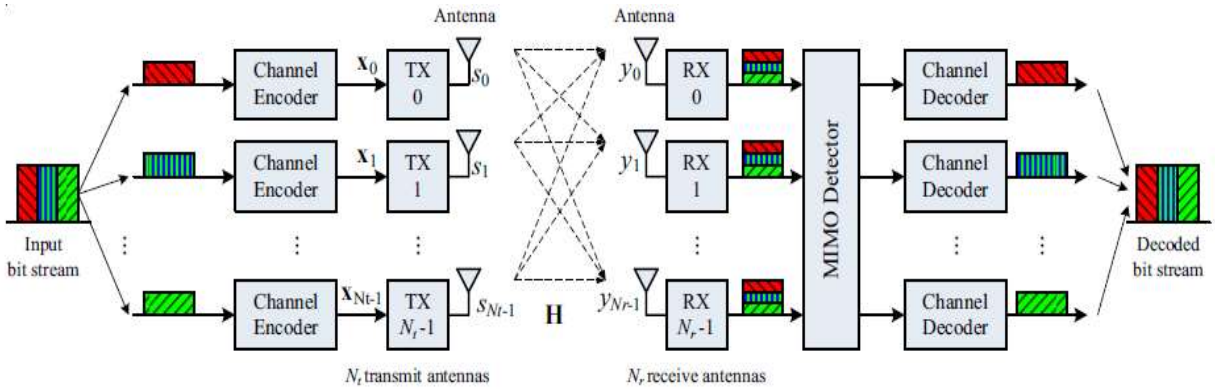


Figure 1: Schematic diagram of MIMO-OFDM transceiver

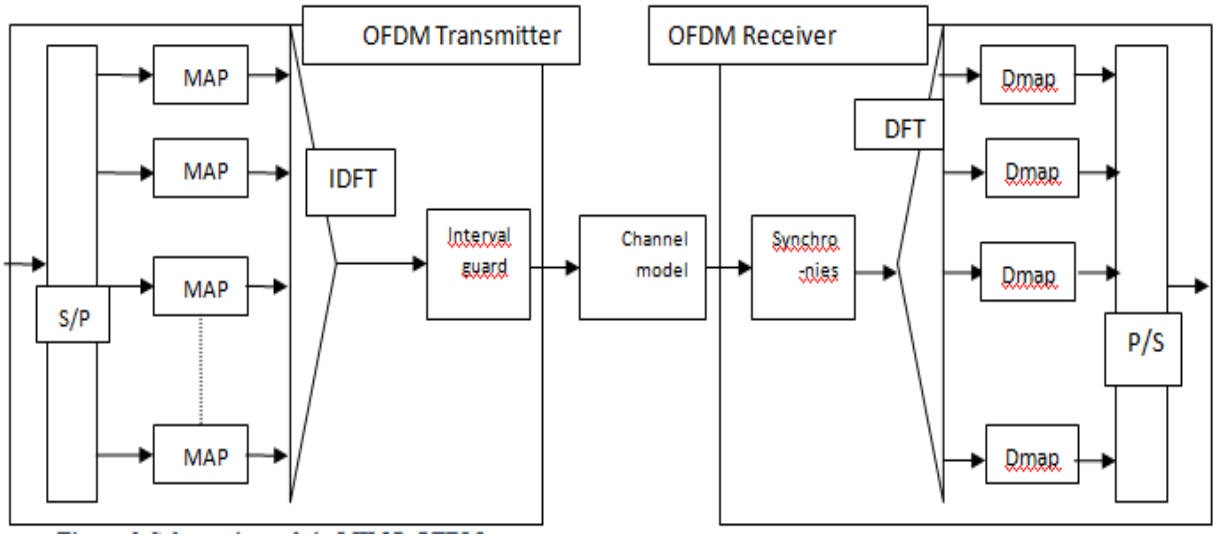


Figure 2: Schematic explain MIMO-OFDM stage processing diagram

3. Detection by multiuser and algorithm proposed

The flow chart below describe the processing signal for encoding and decoding using ICA with SD algorithm, the explanation of flow chart are shown below it.

Step1: Input signal at receiver represent as interference and noise.

$P(y) = P1(kC + y), P2(kC + y), \dots, PCt(kC + y)]^T$ (5)

And $n(y) = [n1(kC + y), n2(kC + y), \dots\dots, nCr(kC + y)]^T$ is additive white Gaussian noise (AWGN).

Step 2: Value fitness evaluate, calculate fitness value in delay and phase.

The calculated estimation delay by:

$\text{đ}_y = arg\,max\left(\left|\sum_{k=1}^{C_M \times C_E} Re(p_y(k).E_y(k)^*\right| + \left|\sum_{k=1}^{C_M \times C_E} Im(p_y(k).E_y(k)^*\right|\right)$ (6)

Where đ_y is estimation delay, Im(.) and Re(.) is imaginary and real part respectively of numbers complex, (.)* represent numbers complex operator conjugate and C is the number of symbols pilot.

The estimation phase can be calculated by:

$\Theta_y = ang\,(\sum C_E p_y\,(t)\widetilde{E_y}(k)^*)$ (7)

Where $\widetilde{\mathrm{E_y}}$ is vector column length $\mathrm{C_M} \times \mathrm{C_E}$ and $\widetilde{E_y} = [E_y(1), \dots, E_y(1), \dots, E_y(C_M), \dots, E_y(C_M)]^T$

$\mathrm{E_y}$ is the kth vector sequence training user of $\mathrm{C_M}$ symbols pilot and ang(.) is operator number complex angle.

Step 3: The function of fitness depending on estimation of phase and estimation of delay are used for sorted signals where:

$\mathrm{Z_{good}} \rightarrow$ the first half (Z); means the signals without noise and interference.

$\mathrm{Z_{worst}} \rightarrow$ the second half (Z); means the signals with noise and interference.

Step 4: Signal decoding used the value of SNR, below the formula that used for decoded sorted signal.

$\widetilde{\mathrm{SNR}} = \arg\left(\min_{\mathrm{SNR}\in\{\mathrm{SNR_{max}};\mathrm{SNR_{min}}\}} (\mathrm{BER})\right)$

Step 5: The formula below used to calculate the interference coefficient.

$\check{h}_{y,\rho}^{(b)} = \frac{1}{2\times C_m(C+1)} \sum_{t=1}^{C_m(C+1)} P_y\,(t)\check{Z}_\rho^{(b)}(t)$ (8)

Step 6: light absorption coefficient actually is an interference, which is calculated by using interference coefficient in above step, the formula is:

$p_y^{(b)}(t) = p_y(t) - \sum_{y=1}^{y-1} \check{h}_\rho^{(b-1)}\,(y) Z_y^{(b)}(t) - \sum_{y=y+1}^{y} \check{h}_\rho^{(b-1)}\,(y) Z_y^{(b-1)}(t)$ (9)

Step 7: Re-estimated worst signals (Zworst) return to step2 [11].

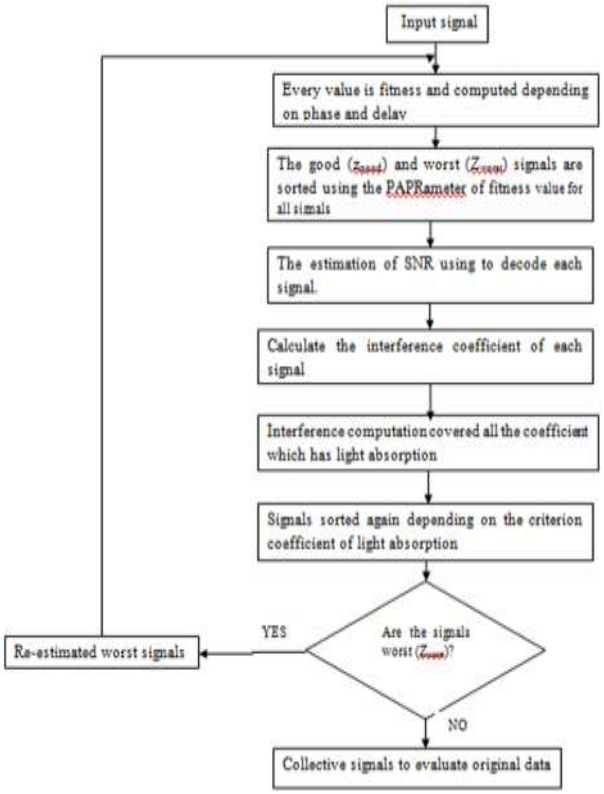


Figure 3: Flow chart for detection by multiuser using ICA with SD algorithm.

4. Implementation of ICA with SD algorithm for MIMO_OFDM system design

In algorithm below, the average moving of signal vectors prior received can be used to estimate matrix F1.The channel matrix S represent estimation channel, so F1 can be evaluated by:

Where F1 – Matrix semi definite.

S- Estimation channel.

SS- vector symbol transmitted of MIMO transmitter

HR - Number of receiver antenna

HT - Number of transmit antenna

Uj(0)s- superscript matrix of transpose conjugate.

T- superscript matrix of transpose.

j- channel coefficient of DFT between receive antenna and transmit antenna.

K- Factor of mutation.Uj(m+1)- Signal with noise and interference.

γ_j −light absorption coefficients

Zj–selection solution perform of jth offspring vectors.

Lj- Block length depending on subcarrier number.
Nj- new value attractiveness of light absorption coefficients.
d- number symbols pilot.
e_d – vector sequence pilot.
(.)* - complex number conjugate.
∗ - Correlation sign.

Fl= $S^S S$, HR≥ HT

=SS^S, HR< HT

And from above can evaluate the pairs(U_j, γ_j)

Given S, H_R , H_T

Fl=$S^S S$, $H_R \geq H_T$

Fl= SS^S, $H_R < H_T$

T=min(H_R,H_T)

Step1: Update and Deflation

For j=1:(T-1)

Starting

$U_j(0)$= subcarrier's adjacent $U_j(\infty)$

$\gamma_j(0)$- $U_j(0)^* U_j(0)$

$Z_j(0) = k/\gamma_j(0)$

Update with j^{th} pair

$U_j(m+1)= U_j(m)+ Z_j(m)(F_j-\gamma_j(m)I)U_j(m)$

Apply deflation

$F_{j+1}= F_j - U_j(m+1)$

End

Step 2: Z_j, L_j, N_j j=1,2,....(T-1) Derivation

If $H_R \geq H_T$

$N_j=\sqrt{\gamma_j}$, $Z_j=\frac{U_j}{\sqrt{\gamma_j}}$, $L_j=\frac{SL_j}{N_j}$

Else

End

Step3:Partial update for Z_T, L_T, N_T

If $H_R \geq H_T$

$N_T=\sqrt{tr(F_T)}$, $L_T=\frac{FT(:,1)}{\|FT(:,1)\|}$, $Z_T=\frac{SL_T}{N_T}$

Else

$N_T=\sqrt{tr(F_T)}$, $Z_T=\frac{FT(:,1)}{\|FT(:,1)\|}$, $L_T=\frac{SL_T}{N_T}$

Step4: Singular vectors of remaining Schmidt

If $H_R \geq H_T$

For d=1:(H_R - H_T)

$U_{T+d}= e_d - \sum_{j=1}^{T+d-1}(e_d, z_j) * z_j$

$N_j=\sqrt{\gamma_j}$, $L_j=\frac{U_j}{\sqrt{\gamma_j}}$, $Z_j=\frac{SL_j}{N_j}$

$Z_{T+d}=\frac{U_{T+d}}{\|U_{T+d}\|}$

else

For d= 1:(H_R - H_T)

$U_j(m+1)^S U_{T+d}= e_d - \sum_{j=1}^{T+d-1}(e_d, L_j) * L_j$

End

- End

5. Methodology Design

FPGA, microcontroller or microprocessor and ASICs all these are methods to carry out OFDM because the OFDM can be implement in digital domain. The system specification executable that shown in Figure 4, explained below:

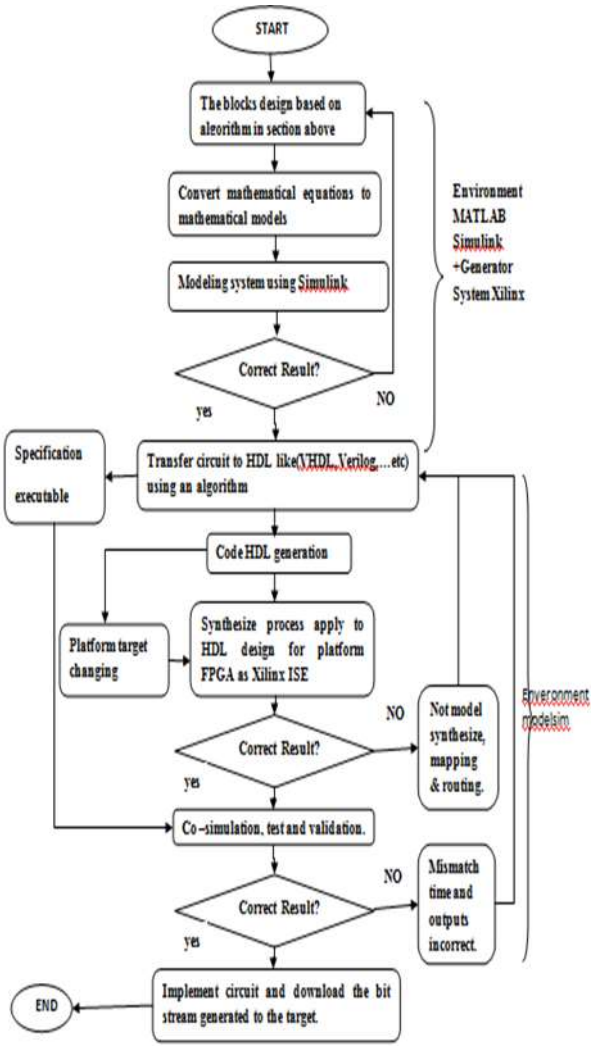


Figure.4: The flow chart diagram explain of model design methodology.

Table 1: System specification parameters

Sample/ Frame construct signal	Frame construct signal
Type arithmetic butterfly	Look up table
Requirement memory	Memory dual port
Samples of slot	15375
Rate sampling (MHz)	30.72
Size IFFT/FFT	2048
Subcarriers occupied number	1200
Blocks resource number	100
Channel bandwidth(MHz)	20
Frequency center	(0.05-6)GHz

Figure.4 shows the diagram of design methodology, regarding implementation of OFDM, FPGA consider is the stellar choice because it gives resilience to the program for the design to reshape beside the cost compared to

other component hardware is low. The basic requirement using Simulink MATLAB, Xilinx ISE 9.2i, Simulink MATLAB that used by each block the algorithm is carried out by use the building in Simulink block diagram. VHDL code is brought in Simulink via set block generator system Xilinx that gives resilience to flow design. Xilinx system generator and Simulink produce true-bit, in the diagram flow design the synthesizer carried out by Xilinx integrated software environment. The blocks simulation hardware check by using modalism via generated vectors test by generator system or benches test HDL. Finally, ISE used to report the blocks results performance and synthesis, the FPGA board pro-gram by generated streams bit.

6. Matlab module Simulation

The module Simulink of the complete transceiver 6x6 MIMO-OFDM represent in Figure 5 that is supported with ICA with SD algorithm. The manual switch used to connect both work Space gateway in and provide from manual switch output the signal as input. The block gateway_innecessary to convert input to Xilinx type from Simulink type. The signal applied to subsystem after connecting to serial to Parallel block. The subsystem encoder and subsystem demodulator that shown in Figure 5 are pictorial in Figures 6 and 7 respectively. Where in Figure 6 shows the encoder carried out in Verilog HDL and integrated to module system. The connection between the reset of the blocks of generator system and encoder, which is located beside buffer Rsc., and buffer/register data blocks. The encoder will process the data where the data information scrambled from encoding and buffer Rsc. block. Buffer small local area used to store encoded bits where the data provided from buffer Rsc. block stop processing by encoder at full buffer. The encoder feedback byte data coded to the block of buffer/ register data when byte data new demand from the block of buffer/ register data. The encoder will avoid jostle data information to the block of buffer/ register data when stop coding. The decoder also carried out in verilog HDL and integrated to module sysgen. Figure 7 shows the processing of decoding after packet detection processing where the decoder take x_rx, y_rx means of I and Q data while byte data decoded generated. The decode data sent to the calculation rate data block for additional processing for checking error. Figure 8 shows the internal design of Mapper processing block Part of the circuit shown in Figure 5, where it contain of 6 RAM4x1 components beside of 6 conversion data type for processing data in transmitter side. The internal design of recovery and demapping block (packet detection) processing in the receiver side shown in Figure 9, the conversion from Simulink to Xilnx or vice versa happened by using the gateways and finally the scope connected to the circuit.

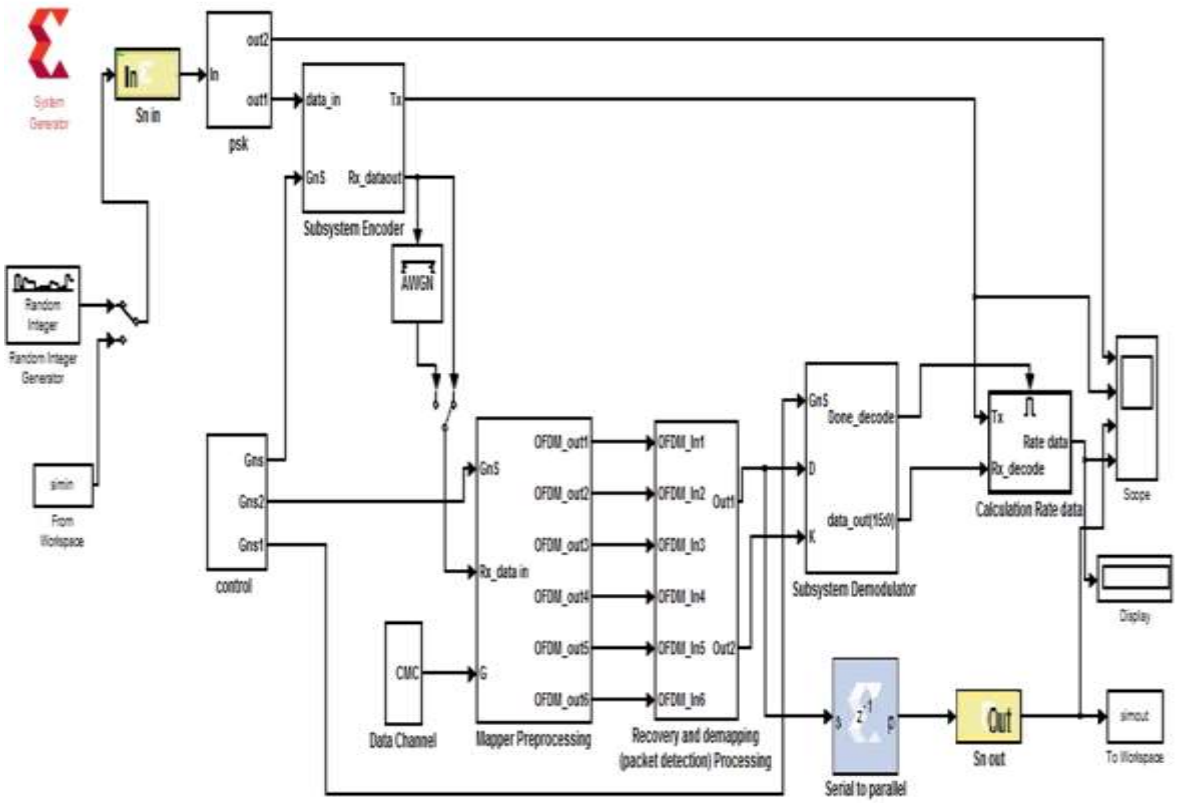


Figure 5: MIMO_OFDM 6x6transceiver module Simulink in matalab.

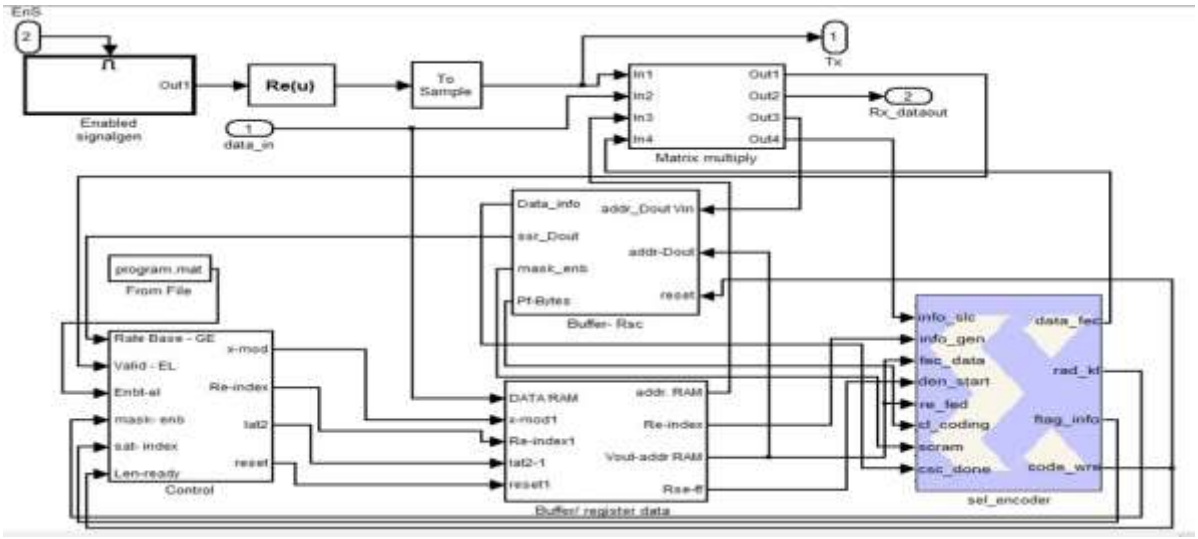


Figure 6: Encoder implemented in verilog HDL for 6x6 MIMO-OFDM model generating system.

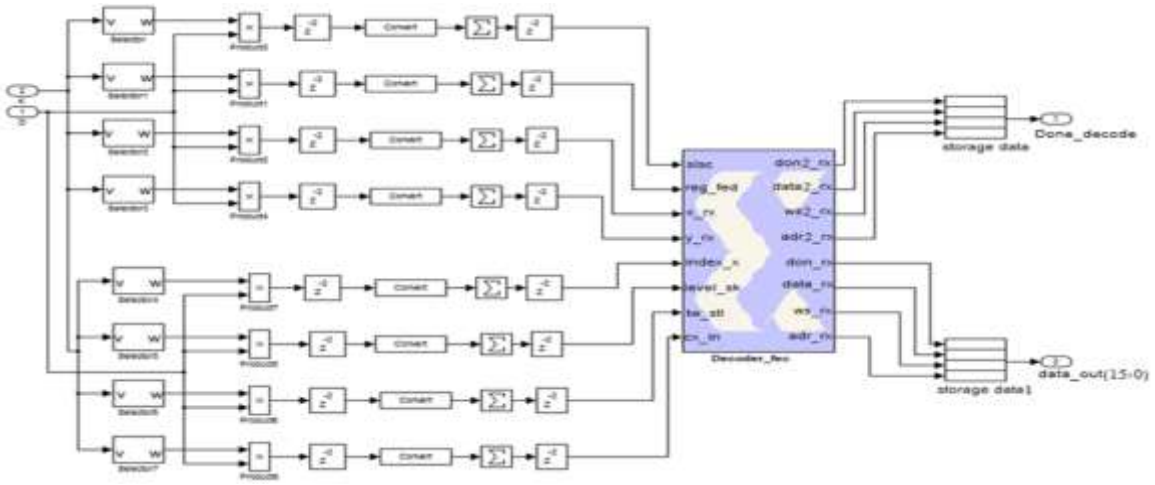


Figure 7: Decoder implemented in Verilog HDL for MIMO-OFDM model generating system.

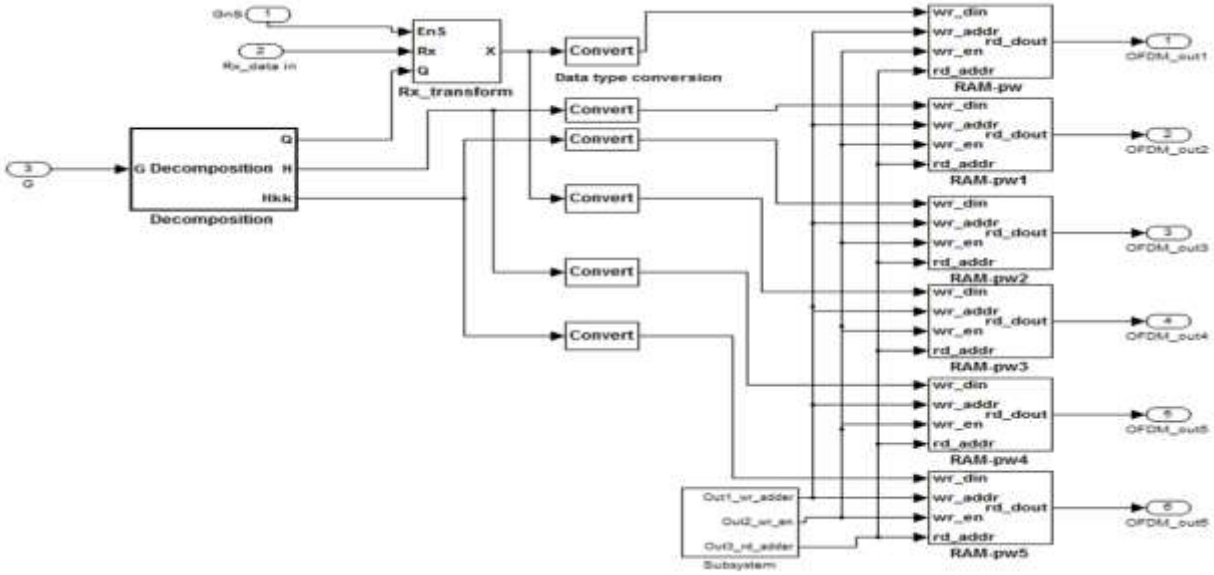


Figure 8: the internal design of Mapper processing block for 6X6 MIMO-OFDM system.

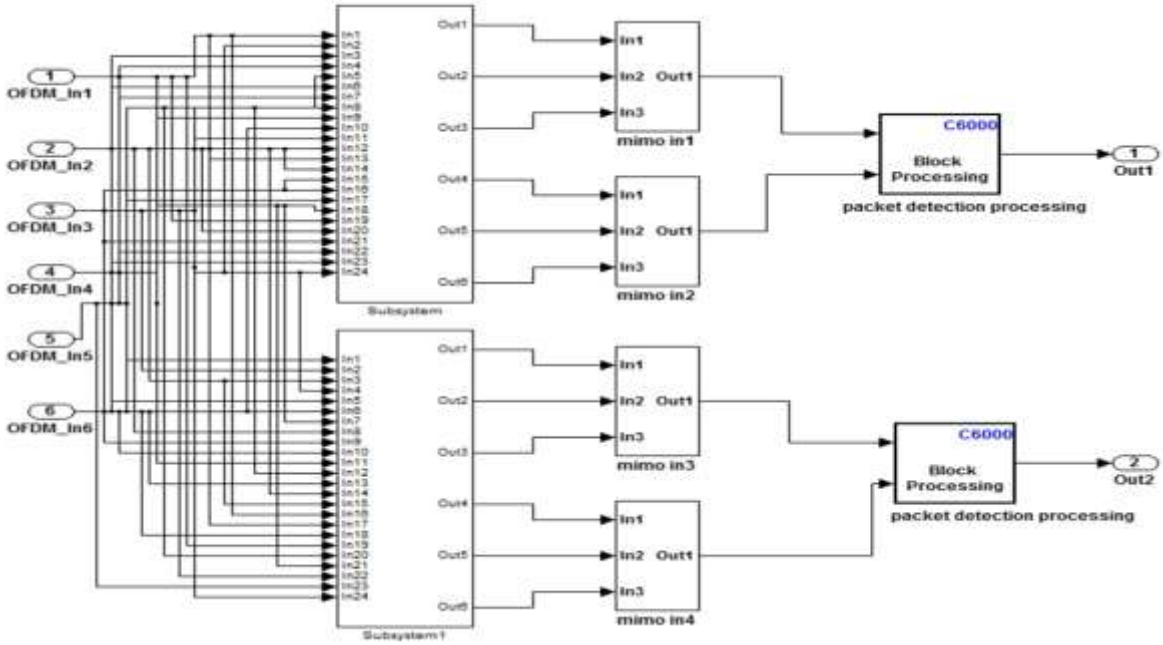


Figure 9: Recovery and demapping block (packet detection) processing in receiver side for MIMO-OFDM system.

7. Simulation results

I. Auricular signal output

Auricular signal that appear in scope is input to the model Simulink, while the signal magnified appears in scope is the signal auricular received as shown in Figure 10 below.

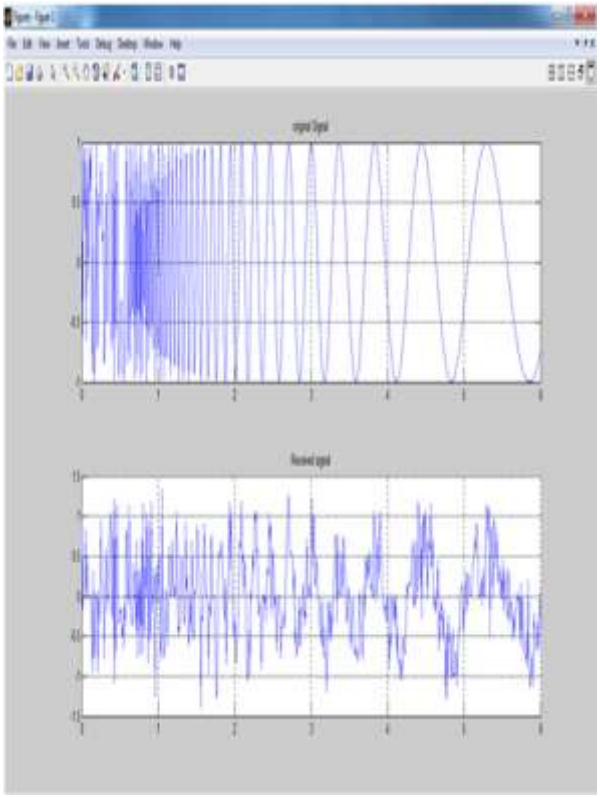


Figure 10: Original and received auricular signal for 6x6 MIMO_OFDM transceiver system

II. Schematic RTL

In the design of circuit digital manufacture, asynchronous circuit digital is models using the abstraction design of RTL (register transfer level), where the data digital signals flux between performed operations logical and registers hardware of signals. The circuit performance of high level can be produced from performance of lower level and at the latest can be derive real wiring by using (HDL) as VHDL and Verilog that supported by RTL as shown in Figure 11 . In newfangled design, digital circuit design by using RTL is perfect applications. The abstraction of level gate logic or level transistor which is called level transfer register usually planed at lower level than the designs of integrated circuit using HDL(Hardware Description Language).The mathematical operations such as else-if-then that are languages program familiar which are constructs to describes the logic integrated as shown in Figure 12 and Figure 13, languages programming computer used from designer to advertise register that depending on variables when implements in HDL. Actually, RTL construct on representation of processing signals in digital integrated circuits. It contains from numbers of slices, Flip-flops, slice LUTs, logic and shift registers components, which are programed in FPGA Spartan-3 XC3S200 using VHDL as in Figures 12 and 13 got internal block of demapper &mapper of 6x6 MIMO_OFDM transceiver respectively.

-a-

-b-

Figure.11: Schematic RTL of 6X6 MIMO_OFDM transceiver by using Verilog with algorithm a- mapper process b- demapper process.

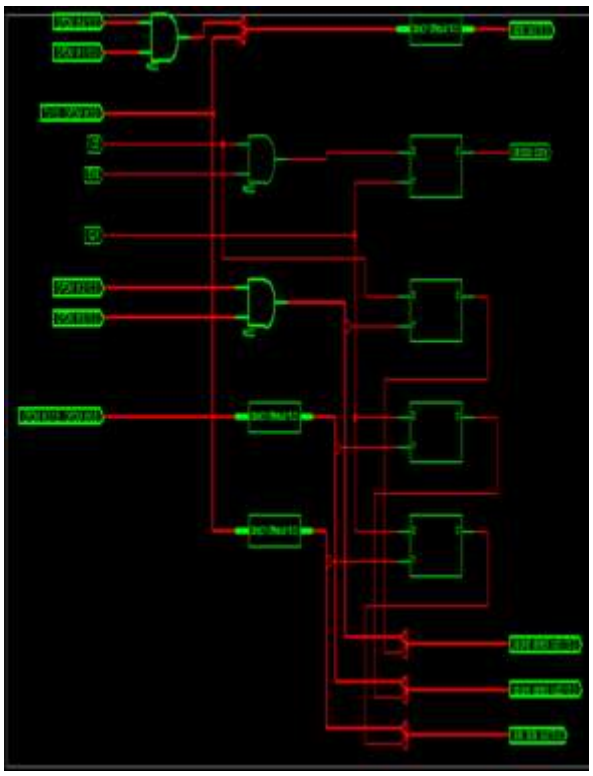


Figure 12:RTL schematic of Internal block of demapper for 6X6 MIMO_OFD

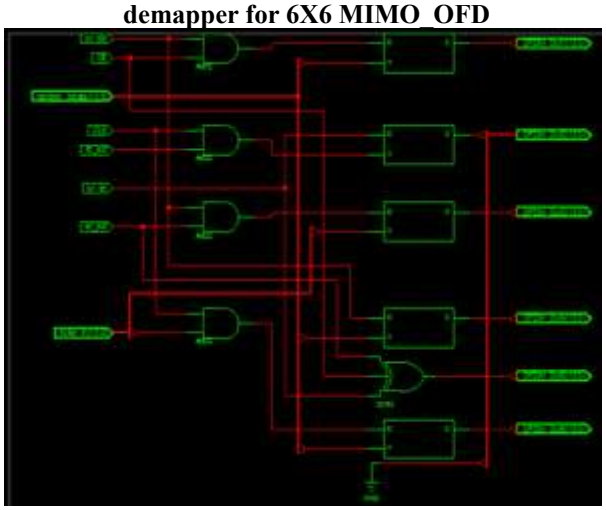
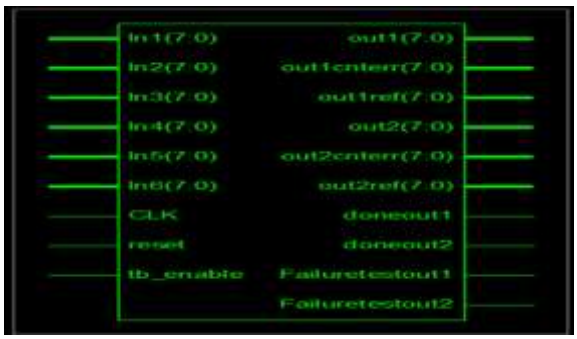


Figure 13: RTL schematic of Internal block of mapper for 6X6 MIMO_OFDM using Vhdl with ICA with SD algorithm

III. Test bench simulation waveform:

In Figure 14, generating test bench of JTAG contains FPGA co simulation of an image input, which are; explain the block of packet detection and its waveform simulation by using VHDL with ICA with SD algorithm.



-a-

-b-

Figure 14: packet detection simulation using VHDL of FPGA on JTAG with algorithm –a-block, b-simulation waveform.

IV.FPGA design summary

The implementation of MIMO_OFDM 6x6 by using FPGA Spartan 3 XC3S200 with combined ICA with SD algorithm, the following results got as shown in fig.15 where the utilization device used 70% slice of flip flops, 55% slice of LUTs, 67% of memory and 37% number of logic.

V. The reduction of PAR using ICA with SD algorithm

In Figure 16 it can be seen clearly the PAR probability comparison between two cases on case using K-BEST algorithm and second case using with ICA with SD algorithm. Where by using K-BEST algorithm the probability of PAR constant until reach 6db and after decrease gradually till 20db at 0 PAR probability. While the PAR probability for the second case by using ICA with SD algorithm the probability of PAR constant till reach 2 db and after decrease gradually till 14db at 0 PAR probability. The reduction of PAR for two different levels achieved for both techniques.

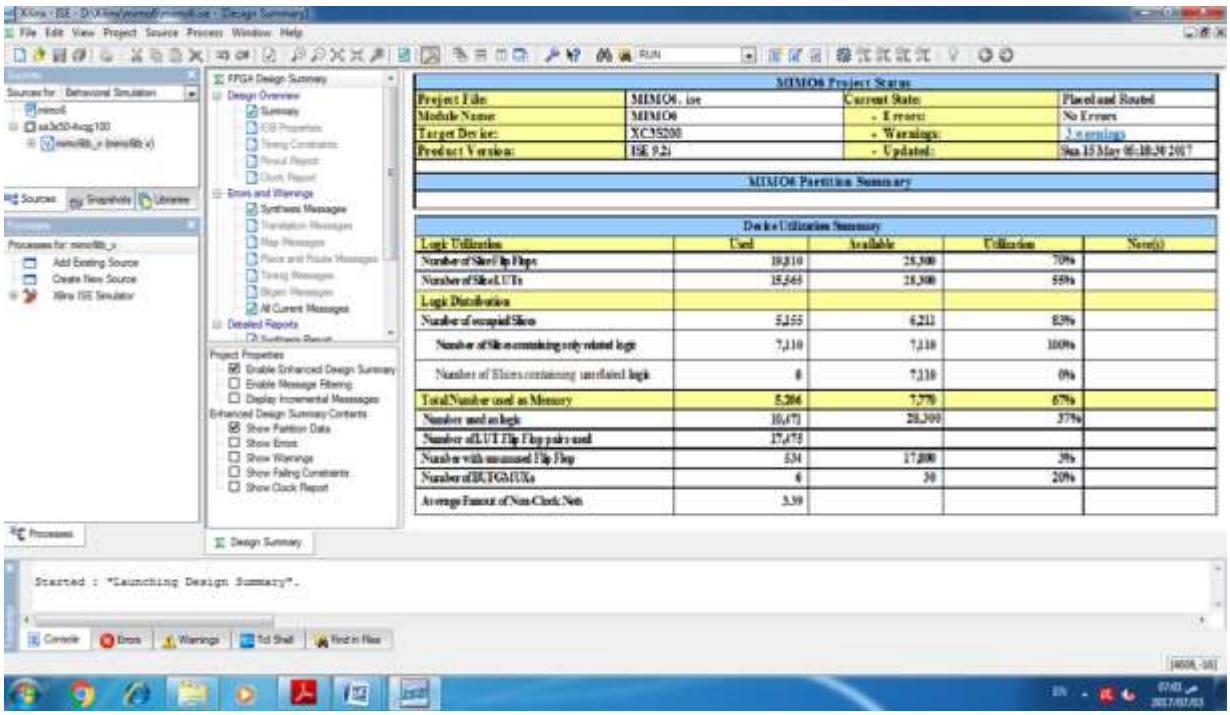


Figure 15: Design summary of utilization device.

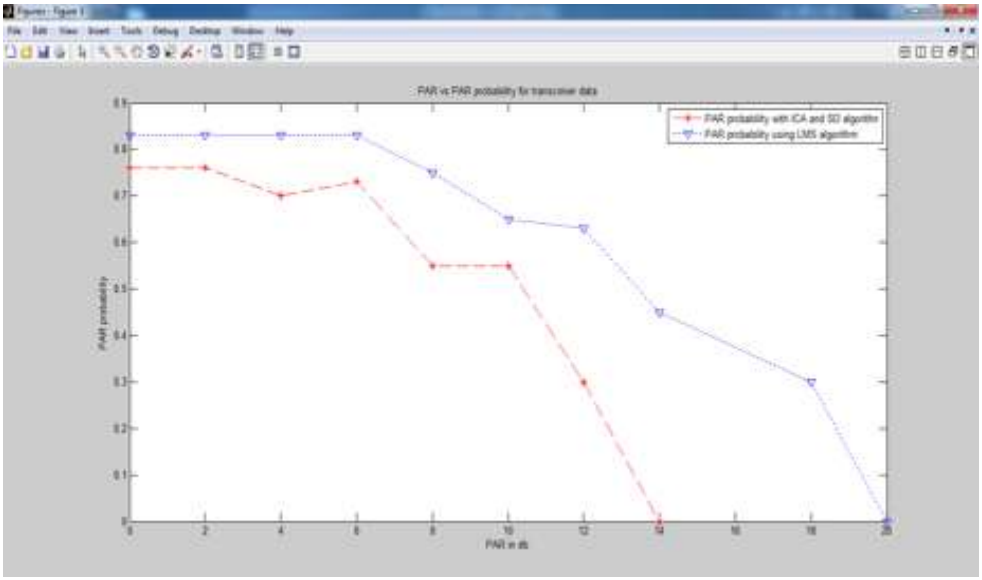


Figure 16: PAR probability vs PAR in dB comparison by using two algorithms K-BEST and ICA with SD algorithm

8. Results Conclusions

It can be seen clearly from table-3 the comparison of this work with two different works for multiple parameters algorithm, technology, Iteration number,Memory, max. frequency and max. throughput. The mean result got maximum throughput 425Mbit/sec. using ICA with SD algorithm is the best result in this research compared with two other previous works 216 Mbps and 365Mbps using Depth-first and K-BEST algorithms respectively, so we got high processing data rate.The main objective of implementation MIMO-OFDM transceiver in FPGA is for the purpose of data transfer at high speed taking into account the cost of implementation hardware as in mean requirements. PAR reduction that using ICA with SD algorithm achieved reduction about 6db compared by using K-best algorithm, where it is obtained high speed data rate about 425 Mbps by using QPSK at 1/2 rate code using spatial technique. The Xilinx ISE 9.2i used for simulation software, then tasted using Spartan 3 XC3S200the results obtained were stable and actual. Finally, the device used 70% slice of flip flops, 55% slice of LUTs, 67% of memory and 37% number of logic.

Table2: PAR probability vs PAR in db by using K-BEST and ICA with SD algorithms

PAR(db)	0	2	4	6	8	10	12	14	18	20
PAR probability using K-BEST	0.83	0.83	0.83	0.83	0.75	0.65	0.63	0.45	0.3	0
PAR probability using ICA with SD	0.76	0.76	0.7	0.73	0.55	0.55	0.3	0	0	0

Table 3: Architecture comparison this work with two different work.

	This work	Howland [1]	Cavallaro [10]
Algorithm	ICA with SD	Depth_First	K-BEST
Technology	65nm	65nm	65nm
Iterations number	11	15	22
Memory(SRAM) (bit)	78,430	77,216	69,122
Maximum Frequency(MHz)	390	246	390
Maximum Throughput (Mbit/sec.)	425	216	365

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