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FPGA-Based Single-Phase PV Inverter Using Unipolar and Bipolar SPWM Control Techniques

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HIGHLIGHTS

- Investigation of FPGA-based SPWM generator as a control mechanism for a PV/Battery full-bridge inverter
- The unipolar SPWM technique produces less harmonic distortion than the Bipolar method, with THD 45% lower
- The system implementation of SPWM Pulse generation has been validated on Xilinx Spartan 6 FPGA (XC6SLX45) board using VHDL code.

ARTICLE INFO

ABSTRACT

The study presents circuitry modeling and methodology to integrate solar photovoltaic (PV) energy with grid (AC) sources to supplement household appliances during a power cut-off or restricted supply period and alternating charge deep cycle batteries. This paper discusses an FPGA-based Sinusoidal Pulse Width Modulation (SPWM) generator as a control mechanism for a PV/Battery full-bridge inverter. The inverter's efficacy is expressed as the Total Harmonic Distortion (THD) ratio, which must be as low as possible. Various schemes are proposed to reduce THD to generate a more sinusoidal output wave. SPWM is mostly used in industrial inverters. Two SPWM techniques, Bipolar and unipolar, are compared under a variety of Modulation Index (MI) conditions and Carrier Frequency (fc) to analyze the best performance of the full-bridge inverter with less (THD) and smoother output sinewave. The present paper discusses the results of a simulation for a single-phase full-bridge inverter employing bipolar and unipolar SPWM techniques. The output waveform demonstrates that the Unipolar SPWM technique produces less Total harmonic Distortion than the Bipolar method, with THD 45% lower. ISE 14.7 and Matlab 2019 are used to present, simulate SPWM generating code, and implement the design on a field-programmable gate array (FPGA), which acts as a controller for the Mosfet gates in the full-bridge inverter to constitute a sine wave without changing any hardware configuration in the circuit design. The system implementation of SPWM Pulse generation has been validated on Xilinx Spartan 6 FPGA (XC6SLX45) board using VHDL code. The final test on the system design for the SPWM generation program, after synthesis and compilation were finalized and verified on a prototype system.

1. Introduction

Solar energy is seen as one of the cleanest, most abundant renewable sources of energy for the future of power generation. Furthermore, with the rapid growth of the populace in urban, suburban, and provincial sectors, the essential requirement of alternative electrical energy is continuously growing.

An inverter is a type of electrical equipment that converts a Direct Current source (DC) from (PV panel or Battery) to an alternating current source (AC). Inverters can be configured in half bridge or full bridge topologies, depending upon the design of the power electronic switches. The full-bridge structure is shown in Figure 1, which consists of two sections, each equipped with two Mosfet switches. The center points of the sections are linked throughout the transformer that supplies power to the load. The gates are controlled by PWM signals through a Xilinx FPGA board.

This paper compares the performance of Unipolar and Bipolar SPWM switching systems using Matlab-Simulink simulations on an H-bridge single-phase inverter. The modulation index (MI) and its varying effects on the resulting inverter output's THD content are investigated. Compared to a bipolar inverter to a unipolar inverter, the output presents a more precise sinusoidal waveform with reduced Total Harmonic Distortion (THD). A unipolar PWM-triggered inverter produces the best sinusoidal output signal [1]. It is noted that Full bridge Unipolar SPWM is more efficient, has lower switching losses, and lower Total Harmonic Distortion (THD). Hence, it enhances power quality and simplifies the filtering process, giving a smoother sinusoidal output waveform than the bipolar inverter [2].

2. Related Works

SPWM modulation control techniques in inverter systems have gained increasing attention for their low cost and less hardware complexity. Many studies have documented in connection with single-phase, three-phase PV inverters using SPWM control techniques and some previous studies that discussed Total Harmonic Distortion of the output current and voltage of the FPGA-based inverter. Baroi, Samanta, and Banerjee examined many types of inverters and their output waveforms, including square wave and SPWM inverters. The outputs of the SPWM inverter are analyzed using the Fast Fourier Transform (FFT) technique. Also, Variation in THD is presented as a function of Modulating Index and Carrier Frequency. The research demonstrates that as the Modulating Index increases, the THD decreases. As a result, this conclusion may be applied in the hardware design of Sinusoidal PWM inverters with the benefit of reduced THD [3].

Bajpayee et al. compared the FFT performance of three distinct inverting designs triggered using sinusoidal pulse width modulation (SPWM). FFT analysis is used to analyze SPWM-based Unipolar and Bipolar inverter topologies. It is observed that the sinusoidal performance of bipolar inverters employing SPWM is superior to that of other comparable switches. The primary objective is to deal with high voltage applications. Isolated-Gate Bipolar Transistor (IGBT) is ideal because of its increased speed and capacity [4]. Alhamrouni et al. had offered a single-phase PV inverter with a sinusoidal pulse width modulation (SPWM) and a low pass filter linked between the inverter and the grid-connected utility to reduce harmonics generated by renewable energy sources. To adjust the magnitude and frequency of the output voltage, both unipolar and bipolar switching schemes are used. Matlab/Simulink is used to simulate the suggested methodology. Through analysis of the simulation results, it was determined that in comparison to the bipolar switching system, the unipolar switching method generates a more sinusoidal and smooth output waveform with less harmonic distortion. However, bipolar switching provides a lower power grade than unipolar switching [5].

Hassaine and Bengourina designed a grid-connected solar system. The main objective is to control the quantity of electricity generated by the solar generator, injected into the grid by the inverter, increasing the photovoltaic system's efficiency. The quality of electricity fed into the grid and the converter system's performance is dependent on the inverter's current regulation. For a solar system connected to the grid, a control method based on Digital Pulse-Width Modulation (DSPWM) is proposed to synchronize a sinusoidal output current with the grid voltage and modify the power factor. This control is based on a bipolar PWM controlled single-phase inverter with a lineal current control. This controller is programmed digitally using VHDL and executed on a Field-Programmable Gate Array FPGA. Digital current control demonstrates the suggested SPWM method's capabilities and simplicity of digital implementation. This method can significantly increase the power quality for the outputs of grid-connected photovoltaic inverters while also lowering the equipment costs associated with these systems [6].

Sarker, Datta, and Debnath [7] suggested a sinusoidal pulse width modulation FPGA-based generator design with configurable modulation index, high frequency, high-resolution digital that meets the requirements for MI adjustment, and high-frequency switching in voltage-source inverter systems. The MI is regulated using a mathematically optimized FPGA architecture by varying the duty-cycle values of the pulses generated by the SPWM in response to the measurements at the inverter output. The laboratory setup was utilized to conduct simulations and tests to demonstrate the proposed FPGA-based architecture fundamentally capability of regulating the MI modulation index value of the SPWM generation for a Voltage-Source Inverter (VSI) application under a variety of input and load conditions. Additionally, the suggested design consumes the fewest FPGA resources, consumes the least power, and has the lowest THD of all previously proposed SPWM methods under consideration. Therefore, the SPWM architecture is the optimal choice for grid-connected inverter applications and variable MI applications due to its superior performance in terms of harmonic distortion, resolution, and power consumption [7].

3. Methodology

3.1 The proposed system design

Figure 2 shows the proposed system design consisting of three inputs (Grid, PV, and battery), an FPGA, full-bridge inverter, and dc to ac rectifier. Three input sources are, PV, Grid, and Battery, are selected according to a priority sequence, which is given by FPGA. The SPWM signals are generated by the Xilinx Spartan 6 FPGA (XC6SLX45) board connected to the driver circuit during PV and battery-working time. When there is electricity from Grid, the system will feed the power directly to the load and charge the battery by a full-bridge AC/DC rectifier. The driver circuit consists of 4 ICs which amplifies the output signals to 15 VDC. The outputs of the driver circuit are connected to the Mosfets' gate terminals. A 12 to 220 AC transformer was connected to the mid legs of the Mosfets. A low pass filter provides a clean sine wave signal then filters the inverter's output.

3.2 Flow chart of the proposed design

Figure 3 shows the flow chart of the system. The priority is given to the AC grid, PV solar, and Battery, respectively. When there is electricity from the Grid, it feeds the house and charges the battery. Otherwise, the system chooses PV when it has sufficient power or Battery to be sent to the inverter's DC source. The FPGA board connected to the driver circuit generates the SPWM signals. This driver circuit consists of 4 TLP250 opto-coupler that amplify and control the FPGA signal to a specific range of 15-volt DC and protect the FPGA board from any short circuit. Then the outputs from the driver circuit are connected to the gate terminal. The inverter's output is then filtered to provide a pure and smooth sine wave signal.

4. Theoretical Foundation

4.1 Sinusoidal Pulse Width Modulation (SPWM)

Sinusoidal Pulse Width Modulation is the most often utilized technique for voltage source inverters in industrial applications (SPWM). The width of the pulses is varied in proportion to the amplitude of a reference signal measured at the pulse's center. When a reference sinusoidal waveform frequency (fr) is compared to a triangular carrier waveform (fc), switching signals are generated. The reference frequency signal (fr) controls the modulation index ratio (ma) by defining the inverter output frequency, peak amplitude, and modulation index. The switching or carrier frequency generates the pulses in every half-cycle. The SPWM inverter operates with a steady DC input and generates sinusoidal waveforms at a specified frequency. For H-bridge inverters, two SPWM methods are available: bipolar and unipolar switching methods. SPWM generation in Bipolar and Unipolar methods is illustrated in Figure 4. The modulation index (Ma) is often referred to as the amplitude-modulation ratio, which is represented in equation (1) [8].
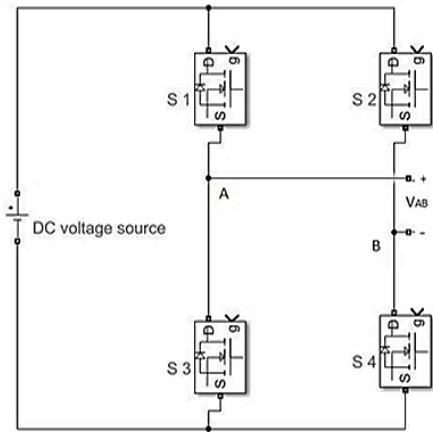

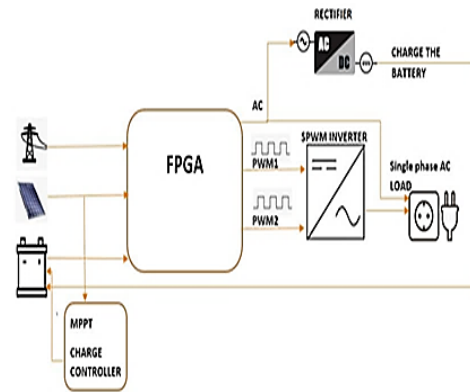**Figure 1:** Single-phase full-bridge inverter Schematic diagram [1]

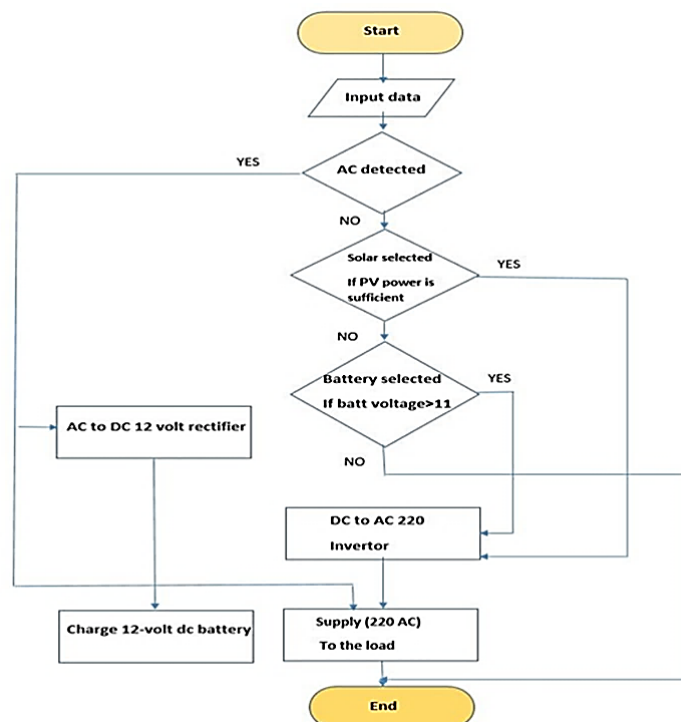**Figure 2:** Proposed system block diagram

Figure 3: Structural flow chart of the design

$$M_a = \frac{V_r}{V_c} \tag{1}$$

Where:

M_a: Modulation index, V_r: Sinusoidal reference, V_c: Carrier triangular wave signal.

    Generation of the digital reference sine wave (Vr) and a triangular carrier wave (Vc) is performed in Matlab, according to a comparison in equation (2) [8].

$$Output_{comparator} = \begin{cases} 1, & if \quad V_c < V_r \\ 0, & if \quad V_c > V_r \end{cases} \tag{2}$$

    The resultant high-frequency harmonics of the SPWM signal are then filtered using a low pass filter, resulting in a high-power and low-frequency sinusoidal waveform Vo at the dc/ac inverter's output terminals. The following equation (3) calculates the amplitude of the output voltage V_0 [9].

$$V_0 = M_a . V_d = \frac{V_r}{V_c} . V_d \tag{3}$$

Where: V_d : Dc input voltage of the dc/ac inverter.

4.2 Switching strategies

    The input data is analyzed mathematically. The intersection of the reference signal and carrier signal creates PWM pulses with periods ranging from n to ßn in each pulse, as seen in Figure 5.

    Each pulse's width at the start and end of each half cycle of the reference signal has the same scale. For example, in the reference signal's positive half cycle, the pulse's width (t1) equals the pulse width (tn) of the previous pulse in the positive half. The period (T) of the reference input frequency (fr) can be calculated in (4). Equations (5) and (6) are used to calculate the switching Angles (αn to ßn) for the beginning and the end of each pulse, respectively, where equation (7) defines the width for each pulse [8].

$$T = \frac{1}{f_r} \tag{4}$$

$$\alpha_n(t) = \alpha_n(°) \frac{T/2}{180^0} \tag{5}$$

$$ß_n(t) = ß_n(°) \frac{T/2}{180^0} \tag{6}$$

$$Width = ß_0 - \alpha_0 \tag{7}$$

Where: T: Time, fr: Reference input frequency, α_n and $ß_n$: Switching angles for the beginning and the end of each pulse, respectively.

4.3 Xilinx Field-Programmable Gate Array (FPGA)

    FPGA is a Field Programmable Gate Array, a part of Programmable Logic Device (PLD) that includes thousands of logic gates. Several of them are connected to make a Programmable Logic Block (CLB). A CLB simplifies the design of high-level circuits. SRAM or ROM provides software linkages between logic gates, enabling the planned circuit to be changed without altering the hardware. Continuous operation, decreased hardware requirements, easy and quick circuit modification, the relatively low cost for sophisticated circuits, and rapid prototyping make it the best choice for prototyping an application with a customized integrated circuit. Figure 6 shows the Xilinx Spartan 6 FPGA (XC6SLX45) board used in this proposed design.

    The clock divider in FPGA divides the 50 MHz clock frequency to get the desired 50 Hz of output sinewave with a desired number of pulses according to the carrier frequency in equation (8). The frequency distribution to calculate the FPGA scale number can be obtained by equation (9) [10].

$$f_0 = \frac{f_s}{n} \tag{8}$$

$$scale = \frac{f_d}{f_s} \tag{9}$$

Where: f_0: Desired output frequency, f_s: The switching frequency, n : Number of sampling pulses, f_d: Frequency of the FPGA board.

4.4 MATLAB simulation

Figures 7 and 8 show the simulation of the SPWM techniques, Bipolar and Unipolar, respectively [10]. The switching angles of the desired pulse width modulation (PWM) for each Mosfet gate are concluded from these Matlab simulations.

Table 1 shows the data obtained for switching angles from Matlab simulation.

The switching data for a Bipolar SPWM was obtained for a 4 kHz switching frequency with a modulation index =1. The data are used in the VHDL programming of the FPGA board to acquire the PWM signals, which controls the gate of the Mosfets.
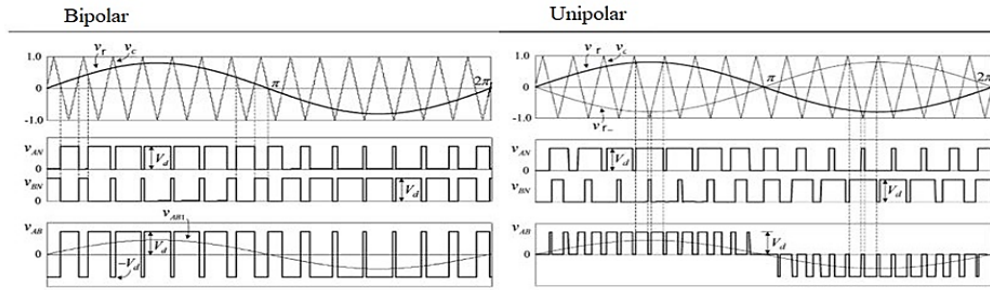

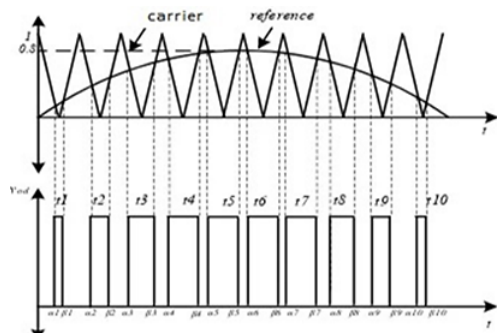**Figure 4:** SPWM generation for bipolar and unipolar [1]

Figure 5: SPWM switching angles [8]

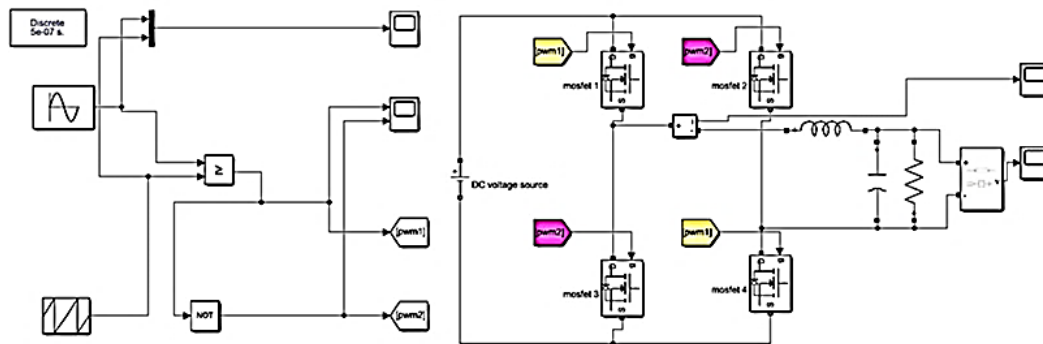**Figure 6:** Xilinx Spartan 6 FPGA board (XC6SLX45)

Figure 7: MATLAB simulation of the full-bridge bipolar inverter
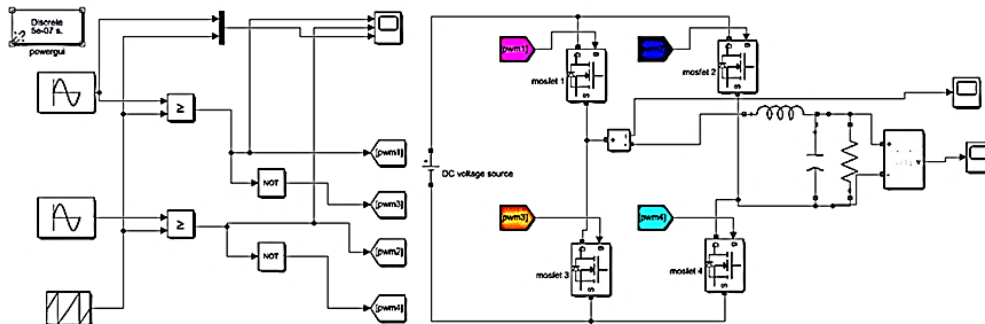

Figure 8: MATLAB simulation of the full-bridge unipolar inverter

5. Simulation Results and Analyses

This project includes two forms of software simulation: circuit simulation using Matlab Simulink (2019) and SPWM pulse generating for the Xilinx FPGA Spartan 6 board using the ISE 14.7 software. The SPWM generator and single-phase full-bridge inverter are designed using Matlab Simulink simulations. The simulation findings are imported into ISE 14.7 and are a reference for designing the hardware component. ISE 14.7 software from Xilinx is used to generate the SPWM in a VHDL (The Very High-Speed Integrated Circuit Hardware Description Language). This simulation process is essential since the ISE 14.7 software's SPWM generating pulse is utilized as the SPWM generator to control the full-bridge inverter circuit. The final generated VHDL code is implemented to Xilinx Spartan 6 FPGA (XC6SLX45) board. All the related waveforms from the simulation are obtained and measured.

Table 1: Switching angles of Bipolar Spwm for fc=4 kHz and modulation index=1

Switching pulses sequence	$\alpha°$	$B°$	$\alpha(t)$ second	$B(t)$ second	Width (t) second
t1	2.25	4.73	0.0001	0.0003	0.0001379
t2	6.74	9.34	0.0004	0.0005	0.0001445
t3	11.23	14.06	0.0006	0.0008	0.0001576
t4	15.72	18.67	0.0009	0.0010	0.0001641
t5	20.21	23.40	0.0011	0.0013	0.0001773
t6	24.70	28.01	0.0014	0.0016	0.0001838
t7	29.19	32.74	0.0016	0.0018	0.000197
t8	33.80	37.35	0.0019	0.0021	0.000197
t9	38.29	41.96	0.0021	0.0023	0.0002035
t10	42.78	46.68	0.0024	0.0026	0.0002167
t11	47.28	51.29	0.0026	0.0028	0.0002232
t12	51.77	55.90	0.0029	0.0031	0.0002298
t13	56.26	60.51	0.0031	0.0034	0.0002364
t14	60.75	65.00	0.0034	0.0036	0.0002364
t15	65.24	69.61	0.0036	0.0039	0.0002429
t16	69.73	74.10	0.0039	0.0041	0.0002429
t17	74.22	78.71	0.0041	0.0044	0.0002495
t18	78.83	83.20	0.0044	0.0046	0.0002429
t19	83.32	87.70	0.0046	0.0049	0.0002429
t20	87.81	92.19	0.0049	0.0051	0.0002429
t21	92.30	96.68	0.0051	0.0054	0.0002429
t22	96.80	101.17	0.0054	0.0056	0.0002429
t23	101.29	105.66	0.0056	0.0059	0.0002429
t24	105.78	110.15	0.0059	0.0061	0.0002429
t25	110.27	114.52	0.0061	0.0064	0.0002364
t26	114.76	119.02	0.0064	0.0066	0.0002364
t27	119.25	123.39	0.0066	0.0069	0.0002298
t28	123.74	127.76	0.0069	0.0071	0.0002232
t29	128.23	132.13	0.0071	0.0073	0.0002167
t30	132.72	136.51	0.0074	0.0076	0.0002101
t31	137.22	140.88	0.0076	0.0078	0.0002035
t32	141.71	145.25	0.0079	0.0081	0.000197
t33	146.32	149.63	0.0081	0.0083	0.0001838
t34	150.81	154.00	0.0084	0.0086	0.0001773
t35	155.30	158.37	0.0086	0.0088	0.0001707
t36	159.79	162.63	0.0089	0.0090	0.0001576
t37	164.28	167.00	0.0091	0.0093	0.000151

Table 1: Continued

Switching pulses sequence	α°	ʙ°	α(t) second	ʙ(t) second	Width (t) second
t38	168.77	171.37	0.0094	0.0095	0.0001445
t39	173.26	175.63	0.0096	0.0098	0.0001313
t40	177.75	180.00	0.0099	0.0100	0.0001248
t41	182.25	184.73	0.0101	0.0103	0.0001379
t42	186.74	189.34	0.0101	0.0105	0.000394
t43	191.23	194.06	0.0104	0.0108	0.0004071
t44	195.72	198.67	0.0106	0.0110	0.0004137
t45	200.21	203.40	0.0109	0.0113	0.0004268
t46	204.70	208.01	0.0111	0.0116	0.0004334
t47	209.19	212.74	0.0114	0.0118	0.0004465
t48	213.80	217.35	0.0116	0.0121	0.0004531
t49	218.29	221.96	0.0119	0.0123	0.0004531
t50	222.78	226.68	0.0121	0.0126	0.0004662
t51	227.28	231.29	0.0124	0.0128	0.0004728
t52	231.77	235.90	0.0126	0.0131	0.0004793
t53	236.26	240.51	0.0129	0.0134	0.0004859
t54	240.75	245.00	0.0131	0.0136	0.0004859
t55	245.24	249.61	0.0134	0.0139	0.0004924
t56	249.73	254.10	0.0136	0.0141	0.0004924
t57	254.22	258.71	0.0139	0.0144	0.000499
t58	258.83	263.20	0.0141	0.0146	0.000499
t59	263.32	267.70	0.0144	0.0149	0.0004924
t60	267.81	272.19	0.0146	0.0151	0.0004924
t61	272.30	276.68	0.0149	0.0154	0.0004924
t62	276.80	281.17	0.0151	0.0156	0.0004924
t63	281.29	285.66	0.0154	0.0159	0.0004924
t64	285.78	290.15	0.0156	0.0161	0.0004924
t65	290.27	294.52	0.0159	0.0164	0.0004859
t66	294.76	299.02	0.0161	0.0166	0.0004859
t67	299.25	303.39	0.0164	0.0169	0.0004793
t68	303.74	307.76	0.0166	0.0171	0.0004728
t69	308.23	312.13	0.0169	0.0173	0.0004662
t70	312.72	316.51	0.0171	0.0176	0.0004596
t71	317.22	320.88	0.0174	0.0178	0.0004531
t72	321.71	325.25	0.0176	0.0181	0.0004465
t73	326.32	329.63	0.0179	0.0183	0.0004399
t74	330.81	334.00	0.0181	0.0186	0.0004268
t75	335.30	338.37	0.0184	0.0188	0.0004202
t76	339.79	342.63	0.0186	0.0190	0.0004071
t77	344.28	347.00	0.0189	0.0193	0.0004005
t78	348.77	351.37	0.0191	0.0195	0.000394
t79	353.26	355.63	0.0194	0.0198	0.0003808
t80	357.75	360.00	0.0196	0.0200	0.0003743

Table 2: Comparative Analysis between Bipolar and Unipolar SPWM inverter with different modulation index

Spwm scheme	Switching Frequency	Fundamental Frequency	Modulation Index	THD% voltage
Unipolar	4 kHz	50 Hz	0.9	0.84
			1	0.68
Bipolar	4 kHz	50 Hz	0.9	1.53
			1	1.28

5.1 Total Harmonic Distortion (THD) comparison in Matlab

Figures 9 and 10 show the %THD analysis with fc=4 kHz, MI=1. Figures 11 and 12 show the %THD analysis with a modulation index of MI=0.9 respectively for both unipolar and bipolar methods, and the results are recorded in Table 2.

5.2 Programming of the Field Programmable Gate Array (FPGA)

After simulation, a VHDL code, which represents the recorded data from Matlab, is generated and implemented to an FPGA board through a USB cable by ISE 14.7 software, shown in Figure 13.

After implementation, the design summary is represented in Figure 14, which shows how many memory slices were used from the total slices available in the FPGA.

The hardware design is constructed, and the VHDL code implementation is accomplished successfully. The hardware design consists of Spartan 6 FPGA (XC6SLX45), an opto-coupler gate driver circuit, a full-bridge inverter circuit, and a sufficient low-pass filter. Figure 15 demonstrates the entire proposed design hardware. Figure 16 shows the output sinusoidal wave illustration with an oscilloscope.
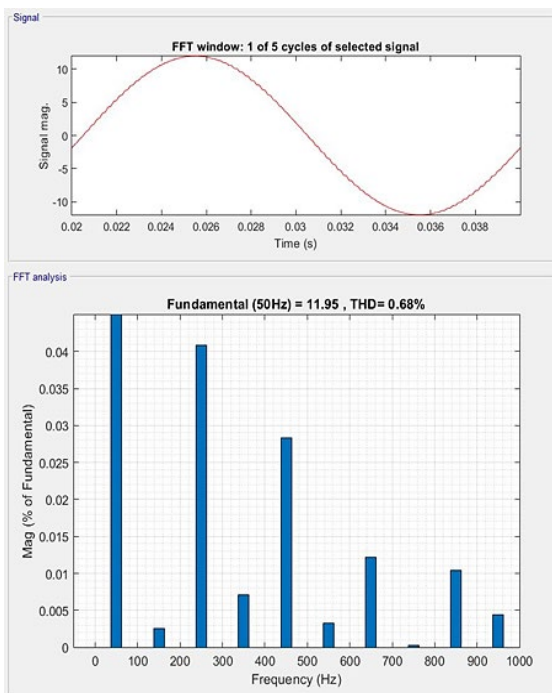
Figure 9: %THD for Unipolar with fc=4 kHz, MI=1
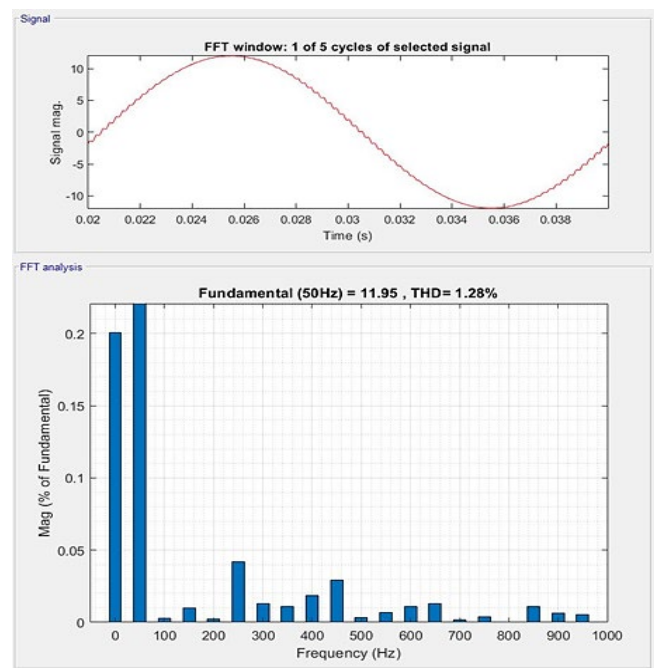
Figure 10: %THD for Bipolar with fc=4 kHz, MI=1

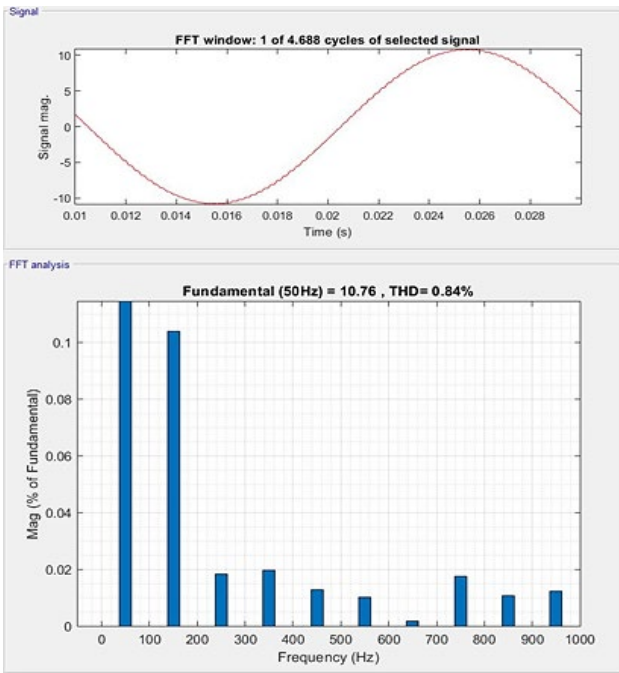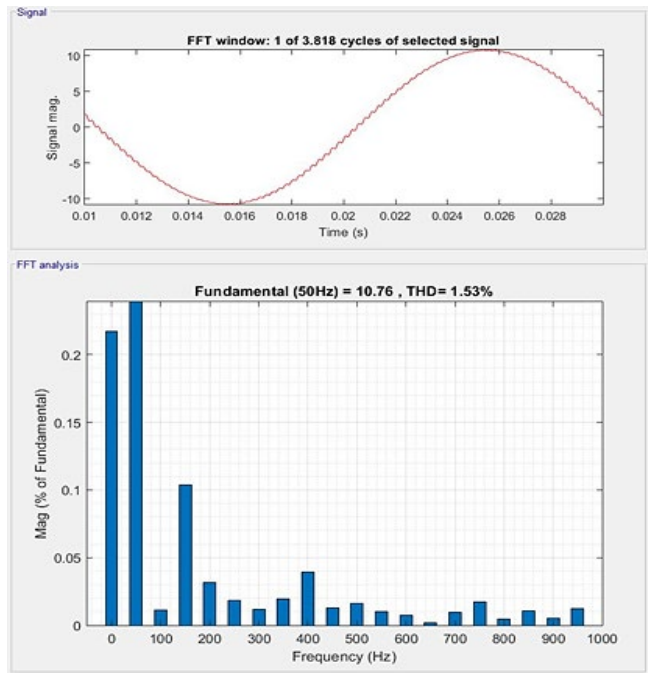**Figure 11:** %THD for Unipolar with fc=4 kHz, MI=0.9

Figure 12: %THD for Bipolar with fc=4 kHz, MI=0.

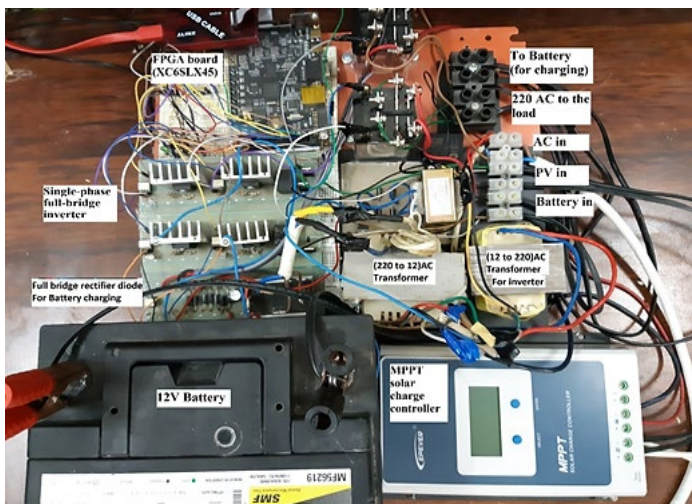**Figure 13:** FPGA (XC6SLX45) programming and implementation
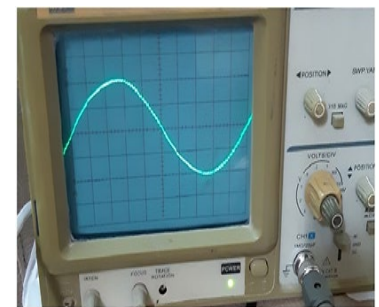

Figure 15: Proposed hardware design

Figure 14: Sinusoidal output with a frequency of 50 Hz, 220 AC

6. Conclusion

The sinusoidal output waveform at the load with 220 VAC and 50 HZ frequency shows that the design of the FPGA-based SPWM PV inverter system has been successful with two SPWM techniques (unipolar and bipolar). The inverter's output voltage

is required to be sinusoidal and configurable in amplitude and frequency, which were represented in the system design by changing the Modulation Index and varying the switching frequency. This paper compared Unipolar and Bipolar SPWM methods with varied modulation indices. The obtained results show that the unipolar scheme has an advantage of a lower percentage of Total Harmonic Distortion (THD) compared to bipolar. According to the Matlab simulation and experimental output data, a unipolar inverter with a sufficient low pass filter circuit produces a more smooth sinusoidal output waveform with lower Total Harmonic Distortion (THD) than a bipolar inverter, with less than (45%). Using an FPGA in the system makes the hardware design simpler and less complex for its high-speed switching up to (MHz) and high resolution. Such a feature allows for flexible adjustment of the planned circuit without modifying the system's hardware, resulting in less hardware easier and faster circuit modification.

Author contribution

All authors contributed equally to this work.

Funding

Data availability statement

The data that support the findings of this study are available on request from the corresponding author.

Conflicts of interest

The authors declare that there is no conflict of interest.

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