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# Study of Power System Load Flow Using FPGA and LabVIEW

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K E Y W O R D S

power flow, FPGA, LabVIEW, monitoring system

A B S T R A C T

*The capability to rapidly execute the power flow (PF) calculations permit engineers in assured with stay bigger assured within the dependability, protection, and economical operation of their system within the case of planned or unplanned instrumentality failures. The purpose of this work is to investigate the use of FPGA characteristics to speed up power flow computing time for the on-line monitoring system of a power system. The work comprises which is the development of the Power flow program using the Fast-decoupled method based on FPGA (Field Programmable Gate Array), and LABVIEW (graphical programming environment). The program delivered very satisfactory results to solve a 30-bus test system. These findings suggest that in general that differences between the proposed work and the conventional fast decoupled method are satisfactory. As for the execution time, because the FPGA uses parallel solutions, the performance of the proposed method is faster. Also, the engagement of the FPGA and the LabVIEW program presented an effective monitoring system for observing the power system.*

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## 1. Introduction

Calculations of power flow are a foundation on which most analyses of the electrical system are based. The power flow calculation results are used to estimate a power system operation under a group, of known cases. The systems are certainly not static and one of the many input cases can be modulated[1]. When the power flow problem is solved for the given operating conditions, we can specify the voltage value and the phase angle δ in each power system bus, which will determine the active and reactive power values in each line. The power injected at each node can be determined, which gives us the value of the active and reactive power loss of the power system[2]. The techniques for solving load flow rely on the iterative solution of the power flow equation such as

Gauss-sidle(GS) , Newton-Raphson(NR)and fast decoupled methods. There are many studies dealt with load flow analysis using various techniques[3][4][5][6]

In power system analysis, many applications are using the FPGA board.in [7], [8], to study electromagnetic transient switching in 3-phase AC machines and power converters for the real-time digital simulator. Also, use the FPGA to analyze the power grid frequency and harmonics signal based on the all-phase FFT spectrum theory. This work used the FPGA (myRIO FPGA) technology to solve the problem of load flow based on the fast decoupled method of LabVIEW's graphical programming environment.

## 2. The Fast-Decoupled Load Flow(FDLF) method

The fast decoupled method is an (NR) modulation that takes advantage of weakly conjugation between P – δ and Q − V due to high X:R ratios[3]. The numerical analysis included in computer-aided electrical energy system analysis is founded on the solution of algebraic equations for execution equations. The first task in the calculation of Power Flow (PF) is to use input data from the transformer and transmission line (TL) to form $Y_{bus}$. The nodal equations for a $Y_{bus}$ power system can be written as follows [9]:

$$I = Y\,V \qquad (1)$$

The nodal equation of the n-bus system may be written in a general form:

$$I_i = \sum_{j=1}^{n} Y_{ij} * V_j \quad \text{for I} = 1,2,3, \ldots,n \qquad (2)$$

The complex power supplied to I bus :

$$P_i + j\,Q_i = V_i * I_i^* \qquad (3)$$

$$I_i = \frac{P_i - j\,Q_i}{V_i^*} \qquad (4)$$

By substituting I in terms Pi and Qi the equation gives:

$$\frac{P_i - jQ_i}{V_i^*} = V_i \sum_{j=}^{n} y_{ij} - \sum_{j=}^{n} y_{i\,j}\, V_j \quad , j \neq i \qquad (5)$$

Equation (2) is written in the polar form in which j includes bus i:

$$I_i = \sum_{j=1}^{n} |Y_{ij}||V_i| \angle(\theta_{ij} + \delta_j) \qquad (6)$$

Active and Reactive power at the bas I is:

$$P_i - jQ_i = V_i^*\, I_i \qquad (7)$$

By substituting Ii in Equation (6) from Equation (7):

$$P_i - jQ_i = |V_i| \angle(-\delta_i) \sum_{j=1}^{n} |Y_{ij}||V_j| \angle(\delta_{ij} + \delta_j) \qquad (8)$$

Separate the actual parts from the imaginary:

$$P_i = \sum_{j=1}^{n} |V_i|\,|V_j|\,|Y_{ij}|\,\cos(\theta_{ij} - \delta_i + \delta_j) \qquad (9)$$

$$Q_i = -\sum_{j=1}^{n} |V_i|\,|V_j|\,|Y_{ij}|\,\sin(\theta_{ij} - \delta_i + \delta_j) \qquad (10)$$

Equation (9) and (10) are a collection of algebraic un-linear equations in terms of voltage magnitude per unit and angle in radians. In Taylor's initial estimate series, equation (9) and (10) develop and the following linear formulas are obtained neglecting all higher-order terms[10].

$$\begin{bmatrix} \Delta P_2^{(K)} \\ \vdots \\ \Delta P_n^{(K)} \\ \Delta Q_2^{(K)} \\ \vdots \\ \Delta Q_n^{(K)} \end{bmatrix} = \begin{bmatrix} \frac{\partial P_2^{(k)}}{\partial \delta_2} & \cdots & \frac{\partial P_2^{(k)}}{\partial \delta_n} & \frac{\partial P_2^{(k)}}{\partial |V_2|} & \cdots & \frac{\partial P_2^{(k)}}{\partial |V_n|} \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ \frac{\partial P_n^{(k)}}{\partial \delta_2} & \cdots & \frac{\partial P_n^{(k)}}{\partial \delta_n} & \frac{\partial P_n^{(k)}}{\partial |V_2|} & \cdots & \frac{\partial P_n^{(k)}}{\partial |V_n|} \\ \frac{\partial Q_2^{(k)}}{\partial \delta_2} & \cdots & \frac{\partial Q_2^{(k)}}{\partial \delta_n} & \frac{\partial Q_2^{(k)}}{\partial |V_2|} & \cdots & \frac{\partial Q_2^{(k)}}{\partial |V_n|} \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ \frac{\partial Q_n^{(k)}}{\partial \delta_2} & \cdots & \frac{\partial Q_n^{(k)}}{\partial \delta_n} & \frac{\partial Q_n^{(k)}}{\partial |V_2|} & \cdots & \frac{\partial Q_n^{(k)}}{\partial |V_n|} \end{bmatrix} \begin{bmatrix} \Delta\delta_2^{(K)} \\ \vdots \\ \Delta\delta_n^{(K)} \\ \Delta |V_2^{(k)}| \\ \vdots \\ \Delta |V_n^{(k)}| \end{bmatrix}$$

Since they are already known, the swing(slack) bus voltage |V| & angle δ is neglected. Jacobian matrix components are obtained after partial equations (9) & (10) derivatives. The equation is written in the form of a matrix:

$$\begin{bmatrix}\Delta P\\ \Delta Q\end{bmatrix}=\begin{bmatrix}J_1 & J_3\\ J_2 & J_4\end{bmatrix}\begin{bmatrix}\Delta\ \delta\\ \Delta|\ V|\end{bmatrix} \quad (11)$$

$J_1$, $J_2$, $J_3$, and $J_4$ are Jacobian matrix components. The variances between the specific values and the calculated values for the terms $\Delta P_i^{(k)}$ *and* $\Delta Q_i^{(k)}$ are called power residuals and are represented as:

$$\Delta P_i^{(k)} = P_i^{(sch)} - P_i^{(k)} \quad (12)$$

$$\Delta Q_i^{(k)} = Q_i^{(sch)} - Q_i^{(k)} \quad (13)$$

The new bus voltage values are:

$$\delta_i^{(k+1)} = \delta_i^{(k)} + \Delta\delta_i^{(k)} \quad (14)$$

$$\left|V_i^{(k+1)}\right| = \left|V_i^{(k)}\right| + \Delta\left|V_i^{(k)}\right| \quad (15)$$

Each iteration has to recalculate the Jacobian matrix terms and the linear equations set in Equation (11). As the planning or operating study usually performs thousands of power flow analyses, Finding ways to accelerate this process was important[11]. The equation's Jacobian matrix (11) is minimized to half due to the negligence of J 2 and J 3 element:

$$\begin{bmatrix}\Delta P\\ \Delta Q\end{bmatrix}=\begin{bmatrix}J_1 & 0\\ 0 & J_4\end{bmatrix}\begin{bmatrix}\Delta\delta\\ \Delta|V|\end{bmatrix} \quad (16)$$

Expanding Equation (16) has two different matrixes :

$$\Delta P = J_1\ \Delta\delta = \left[\frac{\partial P}{\partial\delta}\right]\Delta\ \delta \quad (17)$$

$$\Delta Q = J_4\ \Delta|V| = \left[\frac{\partial Q}{\partial|V|}\right]\Delta|V| \quad (18)$$

$$\frac{\Delta P}{V_i} = -B'\ \Delta\delta \quad (19)$$

$$\frac{\Delta Q}{V_i} = -B''\ \Delta|V| \quad (20)$$

B ' & B " are bus admittance's imaginary components. Ignoring all connected shunt parts is higher, making $J_1$ and $J_4$ easier to form. This can only allow one matrix to perform a repetitive inversion. Successive changes in voltage |V| and angle δ are:

$$\Delta\delta = -[B']^{-1}\ \frac{\Delta P}{|V|} \quad (21)$$

$$\Delta|V| = -[B'']^{-1}\ \frac{\Delta Q}{|V|} \quad (22)$$

## 3. The FPGA architecture

The Field Programmable Gate Array (FPGA) is an array of configurable logic blocks (CLBs) linked through a programmable interconnection network and configurable inputs/outputs [12]. The sum of these parts forms the basic reconfigurable fabric of an FPGA, illustrated in Figure (1). Since the same manufacturing technologies used to make integrated circuits are also used to manufacture FPGAs, FPGAs benefit from a periodic doubling of device density as predicted by Moore's Law. FPGA designers have used these increased resources not only for additional reprogrammable logic but have also expanded CLB functionality, and incorporated high performance fixed function blocks such as binary multipliers, embedded memory blocks, high-speed programmable input/output devices, and fully functional microprocessors into the reconfigurable fabric[13].

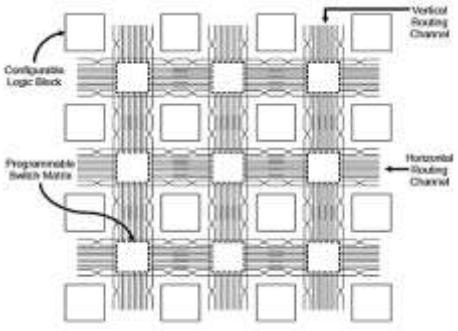


**Figure 1: The FPGA Architecture** [14]

## 4. Structure of the proposed program

The work contains two parts to build the main system as shown in figure (2). The structure of the load flow analysis and the monitoring program, the parts are summarized as follows:

**Part one which contains:**

**1.** Reading the line and bus data (Input data).

**2.** Sending the input data from the host PC using a shared variable to NI-myRIO.

**3.** based on the figure (3) the work will be divided inside the hardware to:

A- A Processor (LabVIEW RT)

- Calculate $Y_{bus}$, B', and B''.
- Invert B' and B''.
- Calculate the power set point.
- Transform data to fixed-point.
- Send this data to FPGA (LabVIEW FPGA) using a shared variable.
- FPGA (LabVIEW FPGA)
- Calculating the Power Mismatch using equations (12) and (13).
- Updating the voltage using equations (14), (15), (21), and (22).
- Checking the convergence criterion.
- Sending the results back to I/O MEMORY table in LabVIEW RT part using the shared variable.
- Sending the results to the HOST PC.

**Part two which contains**

Displaying the results on the screen using the DSC module (Data-logging and Supervisory Control Module).

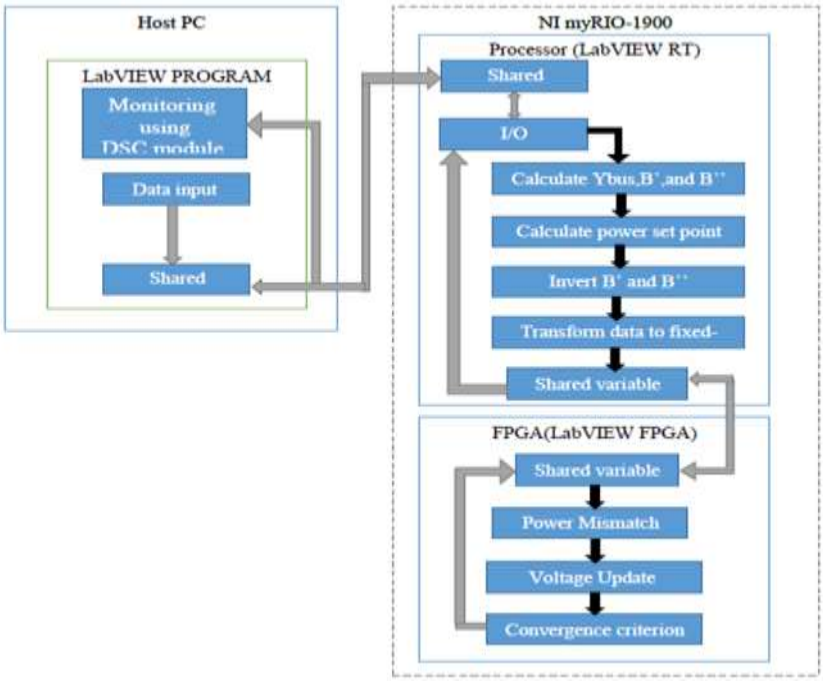


**Figure 2: System Overview Block Diagram**

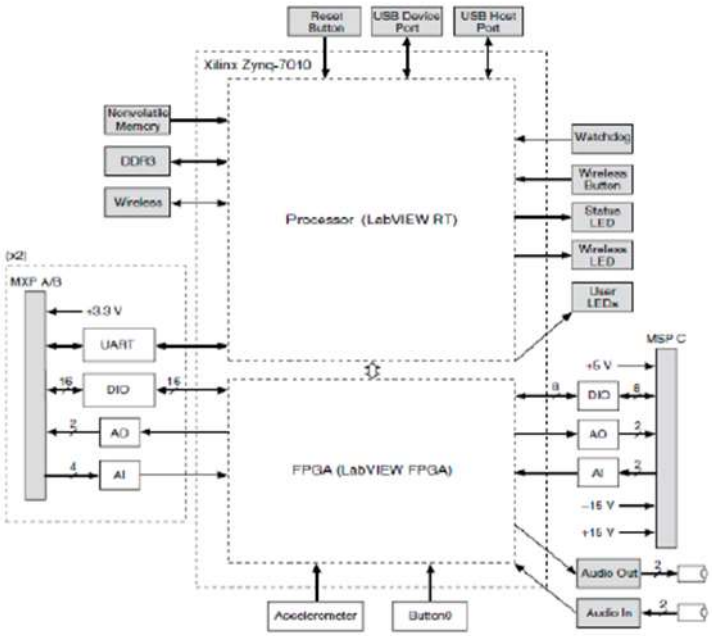


**Figure 3: NI myRIO-1900 hardware block diagram**

The practical aspect of the job includes connecting a personal laptop with the operating system Windows 7 Home Premium, which was configured with the required assistance from LabVIEW. The PC is also used as a monitoring application screen terminal. Figure (4) is the main program connection to the FPGA NI-myRIO.

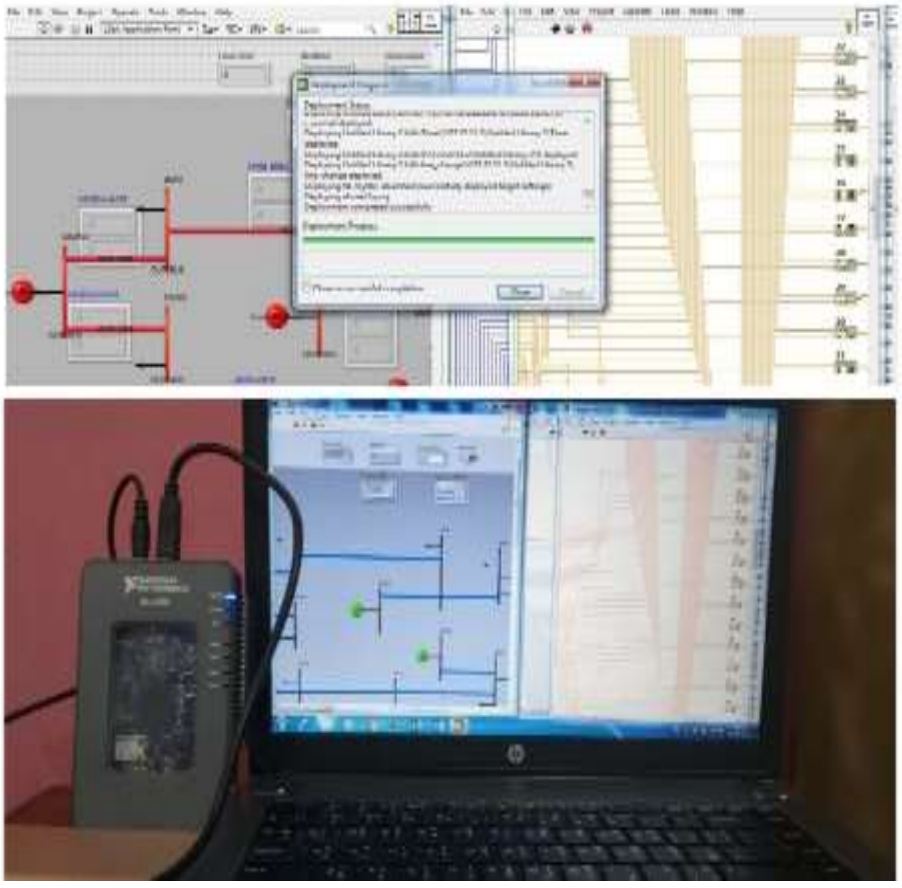

**Figure 4: program connection with the NI-myRIO FPGA**

## 5.Case study

To verifying the effectiveness of the proposed program, it was applied to the IEEE 30-bus test system. All its data are illustrated in the appendix. Figure (5) shows the results of the network built within the program. The program can show the information of any busbar after clicking it as shown in Figure (6). The findings of this study were compared to the findings of reference[15] for the analysis of power flow calculation and were identical. On the other hand, the execution time of the proposed algorithm was compared with a built power flow program using the conventional fast decoupled method and was applied to the test system. The results show that the proposed program execution time was 0.0362191 sec and the conventional MATLAB program execution time was 0.097886 sec. Therefore, the reduction of the execution time was 63%. Which shows the effectiveness of the proposed algorithm.

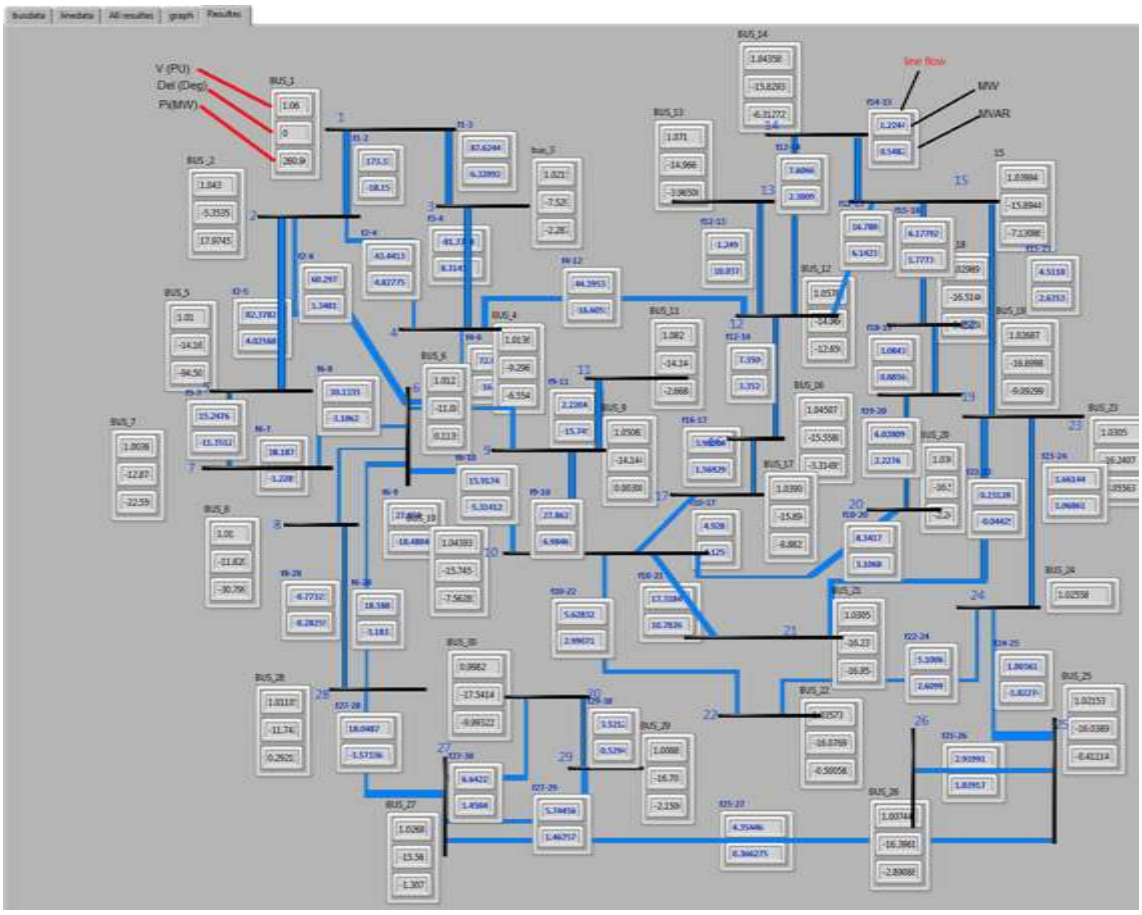


**Figure 5: The IEEE 30 Busbar network is drawing in the program as SCADA**

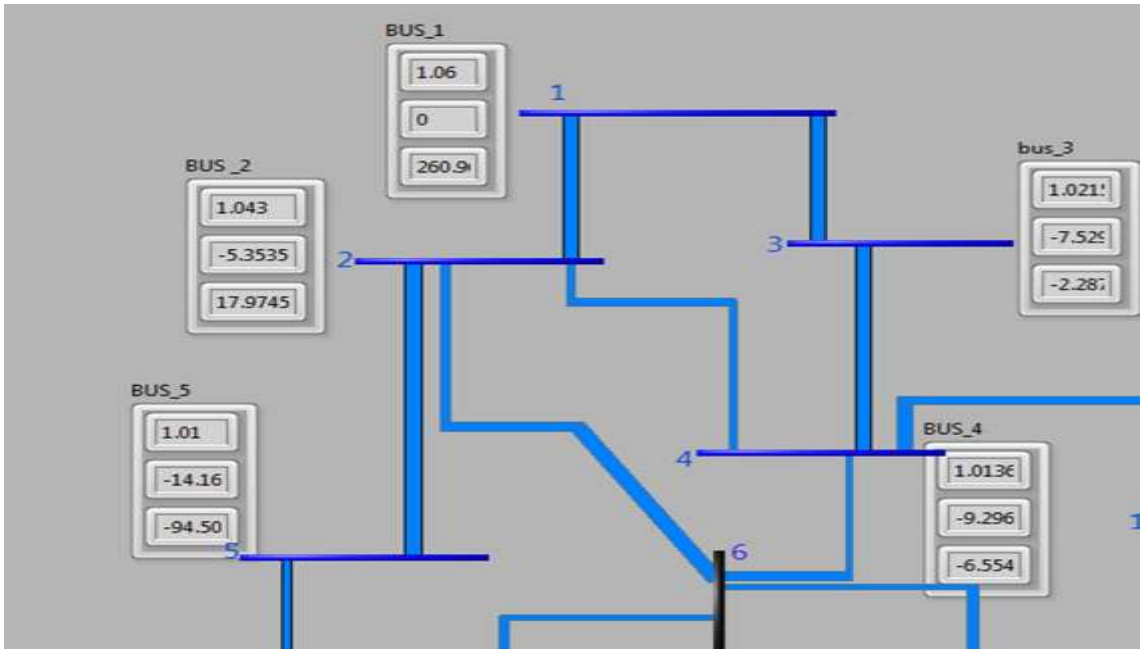


**Figure 6: The result when clicking on the busbar (1,2,3,4, and 5)**

## 6. Conclusions

The current study set out to assess the importance of load flow for the power system. This study set out to calculate the load flow based on NI myRIO-1900(FPGA). The program was implemented in the FPGA using the LabVIEW. The current study found that through the application, the program delivered very satisfactory results to solve a test system of 30 buses. These findings suggest that in general that differences between the proposed work and the conventional fast decoupled method are satisfactory. As for the execution time, because the FPGA uses parallel solutions, the performance of the proposed method is faster. Also, the engagement of the FPGA and the LabVIEW program presented an effective monitoring system for observing the power system.

The proposed work produces a prototype implementation of an FPGA based load flow solver in such a way that the hardware design can be connected directly to the electrical system and the load flow can be converted from off-line application to online application.

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