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An Analytic Design Approach to Inverse Class-F RF Power Amplifiers

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K E Y W O R D S

Class-F^{-1}, GaN HEMT, Harmonic Impedances, High Efficiency, RF Power Amplifier.

A B S T R A C T

The design of high efficiency inverse class-F (class-F^{-1}) radio frequency (RF) power amplifiers includes extensive measurements to characterize the RF power device by means of the empirical load-pull test setup. This paper presents an alternative characterization approach based on evaluating the load impedances analytically at the desired harmonic frequencies for a high electron mobility transistor (HEMT) in terms of the internal and package elements of the active device. It additionally provides a method for extracting the parasitic elements of the power device as well as determining the optimum load-line resistance using the transistor manufacturer's large signal model. A new topology for the output matching circuit is also proposed with its synthetic procedure to present the appropriate harmonic load impedances. To verify this methodology, a 900 MHz inverse class-F power amplifier circuit was designed and its performance was tested with the aid of the Keysight ADS software. The simulation results showed an output power of 38 dBm, a power gain of about 13 dB, DC-to-RF efficiency greater than 87%, and an acceptable level of linearity for both GSM and CDMA modulated signals.

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1. Introduction

Highly efficient RF/microwave power amplifiers are being progressively used in contemporary solid-state radio transmitters to reduce power consumption and increase battery life [1]. The class-E, class-F, inverse class-F, and class-J are among the widely used modes of operation in high efficiency RF power amplifiers. In class-F/F^{-1} power amplifiers, the power transistor is operated as a non-linear current source with certain harmonic terminations at the transistor output. In ideal class F^{-1} power

amplifier, the intrinsic output terminal of the transistor presents a short circuit to all the odd harmonic frequencies (except the fundamental component) and open circuit to the even harmonics. This implies that the drain voltage becomes a half-sinusoidal wave and the drain current approaches to a square wave [2]. However, only a finite number of harmonics are usually tuned in typical class-F^{-1} power amplifiers due to the existence of parasitic components in the active device resulting in significant distortion in the output voltage and current waveforms and an increase in the complexity of the load network [3].

Several works have confirmed that if only the first three voltage and current harmonic components are properly tuned then a DC-to-RF efficiency of greater than 80% can be obtained [4-6]. The optimal values of harmonic load impedances presented to the extrinsic plane of the RF transistor are usually extracted using the load-pull technique in order to maximize the power added efficiency (PAE) of the power amplifier [7,8]. In this contribution, the desired harmonic load impedances are derived analytically as functions of the package parasitic capacitances and inductances using the chip and packaged transistor models. A 6-W power amplifier is then designed and simulated at 900 MHz to confirm the suggested approach using a commercial GaN high electron mobility transistor (HEMT).

2. Characterization of the RF power device for inverse class-F operation

A simplified equivalent circuit model for the RF power HEMT is presented in Figure 1 showing both the intrinsic and extrinsic components [9]. The internal capacitances, $C_{gs,}$ and C_{ds}, are non-linear elements and their values vary with the signal voltage levels at the gate and drain respectively. However, these capacitances are assumed to be constant in this analysis for the sake of simplicity. The drain to source resistance, R_{ds}, is relatively large in the active region and can be ignored. On the other hand, the package parasitic components are very critical at high frequencies and should be estimated from a comparison of the scattering parameters for the bare chip with those of the packaged transistor.

At the virtual drain node (D'), the desired load impedance of the inverse class-F power amplifier for the first three harmonic frequencies is given by:

$$Z_D' = \begin{cases} R_{opt} \ , & for \quad f = f_0 \\ \infty \ , & for \quad f = 2f_0 \\ 0 \ , & for \quad f = 3f_0 \end{cases} \tag{1}$$

where R_{opt} is the optimal large signal resistance at the intrinsic drain plane for the fundamental frequency component, f_0.

The load impedance at the extrinsic drain reference plane (D) differs significantly due to the effect of the parasitic elements of the transistor package. In this case, the load impedance is described as:

$$Z_L = \begin{cases} Z_{L1} \ , & f = f_0 \\ Z_{L2} \ , & f = 2f_0 \\ Z_{L3} \ , & f = 3f_0 \end{cases} \tag{2}$$

where Z_{L1} is the fundamental frequency drain load impedance and is composed from real and imaginary parts where $Z_{L1} = R_{L1} + jX_{L1}$, Z_{L2} is the drain load impedance at the second harmonic frequency and contains only a reactive part where $Z_{L2} = jX_{L2}$, and Z_{L3} is the load impedance for the third harmonic and is given as $Z_{L3} = jX_{L3}$. The second and third harmonic load impedances are purely reactive with no resistive parts in order to prevent power dissipation in the harmonics which is a necessary condition for maximizing efficiency [10].

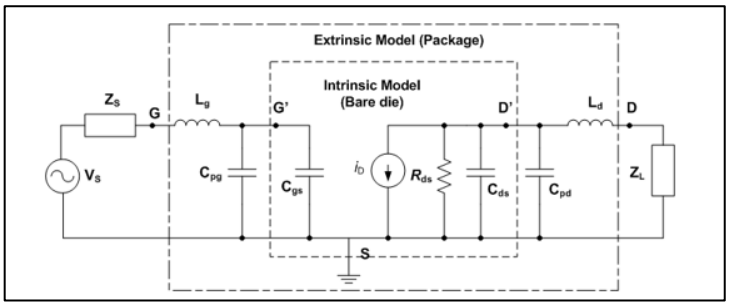


Figure 1: An equivalent circuit model for the power HEMT including intrinsic and extrinsic elements.

The intrinsic capacitance, C_{ds}, is a large signal parameter that does change with the signal level at the virtual drain. However, it can be estimated at the drain bias voltage when the transistor is placed in the cut-off region since its effect is predominant during the OFF time of the RF cycle where the input signal amplitude becomes large enough to drive the FET into the triode and cut-off regions respectively. The typical configuration setup for evaluating C_{ds} is sketched in Figure 2. In this configuration, a signal source is injected at the drain of the bare-chip model and the drain output impedance, Z_d, is simulated over a specified frequency range. The gate is placed at AC ground and the gate-to-source DC bias voltage is maintained below the threshold voltage. The internal drain-to-source capacitance resonates with the drain bias choke at a certain frequency and therefore Z_d is maximized at this frequency so that C_{ds} can be calculated from:

$$C_{ds} = \frac{1}{\omega_r^2 L_1} \tag{3}$$

Where ω_r is the frequency of resonance and L_1 is the inductance of the drain bias choke.

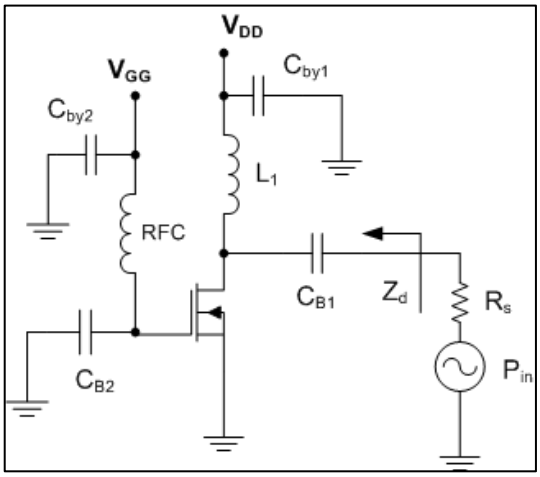


Figure 2: Circuit configuration for evaluating C_{ds}

The dynamic resistance, R_{opt}, is the ratio between the magnitude of the fundamental drain voltage component and the fundamental drain current component at the virtual drain plane (D'), and can be estimated from [11]:

$$R_{opt} = \frac{\gamma_V^2 . V_{DD}^2}{2P_{out}} \tag{4}$$

Where γ_V is the voltage waveform factor and equals to $\sqrt{2}$ for the case of second harmonic open circuit and third harmonic short circuit with all other higher harmonics ignored. V_{DD} is the drain supply voltage, and P_{out} is the desired RF output power.

Alternatively, the optimum load resistance can be determined more accurately from the bare chip model of the active device by terminating its drain with the proper harmonic impedances that present the desired open circuit for the second harmonic frequency and the desired short circuit for the third harmonic frequency while, at the same time, adjusting the load resistance for a specific range. The optimum dynamic load-line resistance is the value at which the power-added efficiency of the circuit is maximized. A typical configuration for such a loading network is presented in Figure 3.

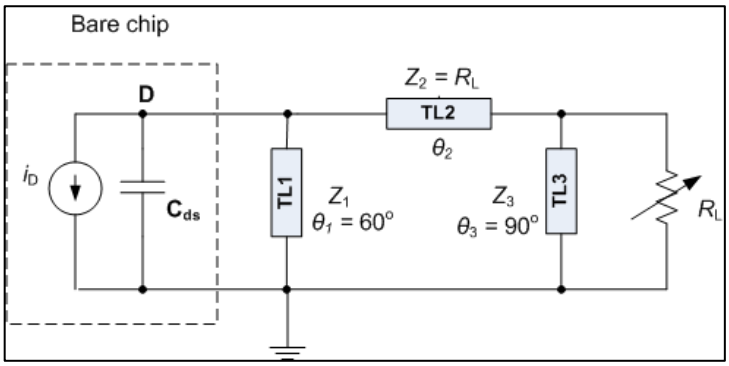


Figure 3: A configuration for the load network used to evaluate the optimum drain impedance

The drain equivalent circuit of the HEMT chip model is simply characterized by a nonlinear current source in parallel with the drain-to-source output capacitance. The short circuited λ/6 stub, TL1, provides short circuit condition to the drain at the third harmonic frequency. However, its impedance is inductive at the fundamental frequency which should tune out the capacitive effect of C_{ds}. Therefore, the characteristic impedance of TL1 can be calculated from the equation below:

$$Z_1 = \frac{1}{\sqrt{3}\omega_o C_{ds}} \tag{5}$$

where ω_o is the fundamental radian frequency.

The series transmission line, TL2, presents the load resistance R_L to the drain at the fundamental frequency since the characteristic impedance of this line equals to R_L. For the second-harmonic frequency, the parallel transmission line, TL3, provides a short circuit to TL2. In this case, TL2 presents an inductive reactance while transmission line, TL1, gives capacitive reactance. The electrical length of TL2 can, therefore, be determined such that TL2 tunes out the capacitive reactance constituted from C_{ds} and the reactance of TL1 at the second-harmonic frequency so as to present an open circuit, and hence:

$$\theta_2 = \frac{1}{2}\tan^{-1}\left(\frac{1}{2\omega_o C_{ds} R_L + \frac{R_L}{\sqrt{3}Z_1}}\right) \tag{6}$$

As long as R_L is varied, the electric length of TL2 is adjusted accordingly. The $\lambda/4$ shorted stub, TL3, presents an open circuit at both the fundamental and third harmonic frequencies, and short circuit at the second harmonic frequency.

3. Derivation of the optimum load harmonic impedances

The optimum load harmonic impedances for inverse class-F power amplifier operation can be estimated in terms of the transistor internal and package elements. If the intrinsic capacitance, C_{ds}, and the extrinsic package capacitance, C_{pd}, are combined in one capacitance, C_{out}, then the equivalent circuit at the output of the RF device can be simplified as shown in Figure 4. The output inductance at the drain refers to the combination of the drain bond wire and strip-line inductances.

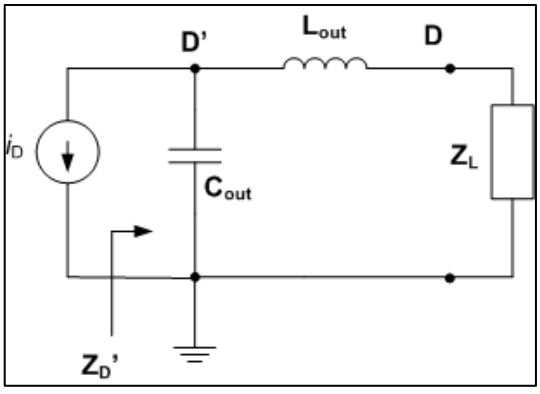


Figure 4: A simplified output network for the HEMT

At the fundamental frequency, $Z_{L1} = R_{L1} + jX_{L1}$, and the intrinsic drain impedance is given by:

$$Z_D' = R_{opt} + j0 \tag{7}$$

It can also be proved that:

$$Z_D' = \left(\frac{1}{j\omega_o C_{out}} \right) \| (R_{L1} + jX_{L1} + j\omega_o L_{out}) \tag{8}$$

Equation (8) can be simplified and re-arranged to isolate its real and imaginary parts. Equating the real and imaginary parts of Eq.s (7) and (8), and solving for R_{L1} and X_{L1} yields:

$$R_{L1} = \frac{R_{opt}}{1 + (\omega_o C_{out} R_{opt})^2} \tag{9}$$

$$X_{L1} = \frac{\omega_o C_{out} R_{opt}^{\ 2}}{1 + (\omega_o C_{out} R_{opt})^2} - \omega_o L_{out} \tag{10}$$

The second harmonic intrinsic drain impedance must be infinite as stated in Eq. (1). Therefore, the combination of the load reactance X_{L2} and the drain parasitic inductance L_{out} should resonate with C_{out}. Thus, the load impedance is purely inductive at the second harmonic and can be estimated from:

$$Z_{L2} = j\left(\frac{1}{2\omega_o C_{out}} - 2\omega_o L_{out} \right) \tag{11}$$

In order to produce a short circuit condition to the virtual drain terminal in the case of the third-harmonic frequency, the load reactance should be capacitive so as to constitute series resonance with the parasitic inductance L_{out}, and therefore:

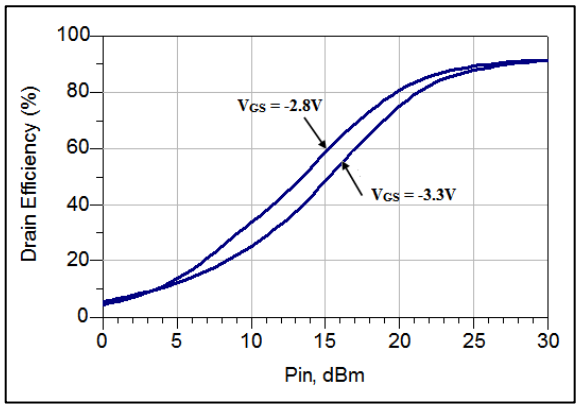
$$Z_{L3} = -j3\omega_o L_{out} \tag{12}$$

4. Design of an Inverse Class-F Power Amplifier Circuit

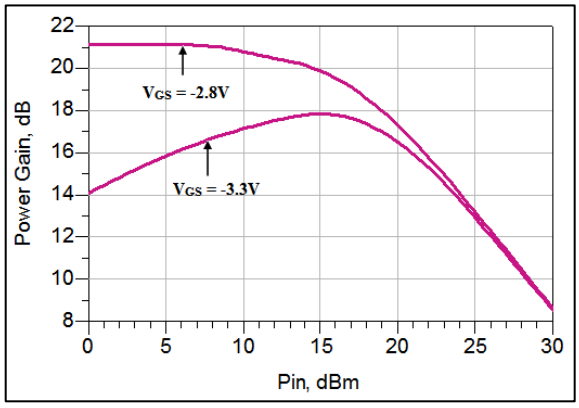
Based on the proposed design approach, a power amplifier circuit was designed and simulated with the aid of the microwave CAD program ADS of Keysight. A commercial 6-W GaN HEMT of Wolfspeed has been chosen in this circuit. This is a broadband RF power transistor that is capable of working up to 6 GHz and has a drain-source breakdown voltage of 120V, making it suitable for inverse class-F operation. The transistor manufacturer delivers both its ADS chip model (CGH60008D) and its ADS packaged model (CGH40006P). The simulated DC characteristics show that the gate threshold voltage is about -3.3V when the FET is operated from a drain supply voltage of 28V.

I. Selection of the bias point

In an inverse class-F power amplifier, the choice of the value of gate bias voltage is very critical on the drain efficiency of the circuit. Some studies proved that a considerable drain quiescent current is necessary to increase the drain efficiency as well as the power gain [12]. This is not similar to the class-F power amplifier where the transistor is usually biased near the threshold voltage [13]. In order to select an optimum bias point, the GaN HEMT bare chip model is loaded with a network similar to that presented in Figure 3 with the optimum load resistance estimated from Equation (4). The performance characteristics of the circuit are swept against the driving power level for several gate-to-source bias voltages. In Figure 5 the drain efficiency and power-gain are sketched against the input signal level for two bias conditions in which V_{GS1} = -3.3 and V_{GS2} = -2.8V. The drain bias current in the first case is about 2 mA, and it is approximately 100 mA for the second bias voltage. It can be seen that both the efficiency and power gain are almost greater in the second case when V_{GS} = -2.8V for low input signal levels. The difference in performance, however, vanishes for the over-drive levels when the active device becomes deeply saturated. Further increase in quiescent bias current does not give much more improvement in efficiency. So, V_{GS} = -2.8V is found to be adequate in this design.



(a)



(b)

Figure 5: Variation of drain efficiency (a) and power gain (b) versus input power for two bias voltages

II. Stabilization circuit

To ensure the stability of the power amplifier, the large signal *S*-parameter simulation is carried out to evaluate the stability factor, *K*, over the specified range of input power level at 900 MHz. It has been shown that the transistor is potentially unstable ($K < 1$) overall power levels. Therefore, a stability circuit consisting of a parallel RC network together with a series transmission line is inserted at the gate terminal to damp out any tendency for oscillation as shown in Figure 6. The resulting stability factor is sketched against input drive power in Figure 7.

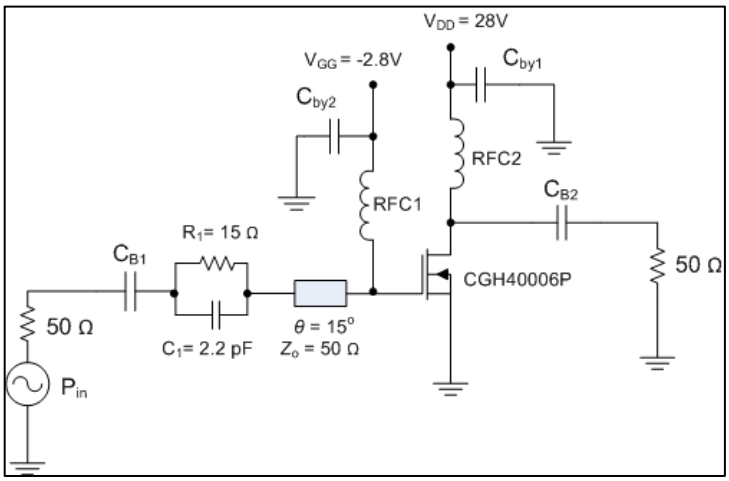


Figure 6: Stabilization network for the power HEMT

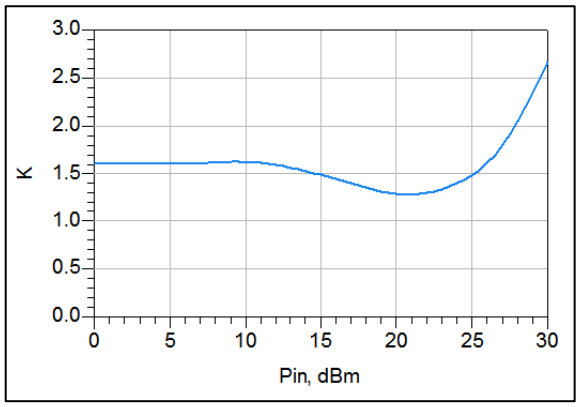


Figure 7: Stability factor versus input power after inserting the stabilization network

III. Determination of the transistor parasitic elements

The parasitic capacitances and inductances of the power transistor can be found by comparing the *S*-parameters of the packaged model with their counterparts of the equivalent two-port network resulting from the bare die model embedded with the parasitic components at the same bias point and frequency range. The ADS optimization capabilities are utilized to minimize the least squares error function based on the *S*-parameters of the two transistor models by systematically varying the inserted elements until the error function approaches zero. The error function is of the form:

$$e = \sum_{f=f_L}^{f_H} \alpha_1 \left| S_{11c} - S_{11p} \right|^2 + \alpha_2 \left| S_{21c} - S_{21p} \right|^2 + \alpha_3 \left| S_{12c} - S_{12p} \right|^2 + \alpha_4 \left| S_{22c} - S_{22p} \right|^2 \quad (13)$$

where S_{ijc}, S_{ijp} are the *S*-parameters of the chip plus parasitics model and the packaged model respectively at the specified frequency, α_k are some weighting factors, and f_L, f_H are the lower and upper band frequencies respectively.

After computer optimization, the values of the parasitic elements are found to be L_d = 0.65 nH, C_{pd} = 0.6 pF, L_g = 0.55 nH and C_{pg} = 0.5 pF as depicted in Figure 7. A comparison between the forward transmission parameter, S_{21}, of the bare-die plus parasitics model and that of the packaged model is presented in Figure 8 shows that the two responses are almost close to each other.

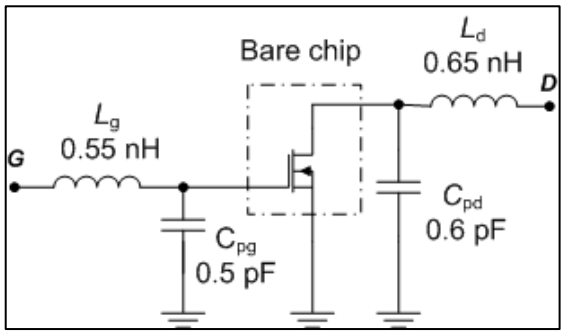


Figure 7: The optimized parasitic elements of the HEMT

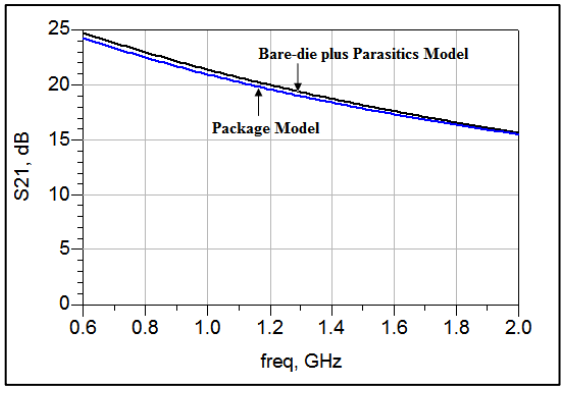


Figure 8: Variation of S_{21} with frequency for the HEMT models

IV. Evaluation of the intrinsic elements

The internal parameters of the transistor are found as illustrated in section 2. The output capacitance C_{ds} of the chip model are estimated from the test setup of Figure 2 where the FET is biased in the pinch-off (cut-off) region. The obtained value is 0.64 pF. On the other hand, the optimum dynamic load-line resistance is estimated from the setup of Figure 3, where a loading network is added to the output of the bare-die model to present R_L at the drain for the fundamental frequency, an open circuit at the second harmonic, and a short circuit at the third harmonic frequency. R_L is changed over a specified range and the output power and drain efficiency are measured accordingly. The parameters of the transmission-line sections that constitute the loading circuit are evaluated from Eq.s (5) and (6) respectively. The schematic diagram of the test circuit used to find R_{opt} is sketched in Figure 9. The stabilization network is inserted at the gate circuit together with a $\lambda/8$ short-circuited bias stub for raising the second harmonic component at the transistor input and thereby to increase efficiency [13]. In Figure 10, both the power-added efficiency and drain efficiency are presented against load resistance, while Figure 11 shows the variation of output power versus R_L. A value of 120 Ω for R_{opt} has been selected as a compromise between maximized efficiency and acceptable output RF power. It is obvious from these sketches that although the output power is maximized when R_L = 40 Ω, the drain efficiency is not optimal for this value of load resistance.

V. Design of the matching networks

In order to synthesize the output matching network, the harmonic load impedances are first calculated as stated in section 3. Substituting for the intrinsic and extrinsic elements of the RF transistor model in Eq.s (9) and (10) gives the load impedance for the fundamental harmonic at the drain, Z_{L1} = 70+j56 Ω. Similarly, from Eq.s (11) and (12) the second and third harmonic impedances at the extrinsic drain are $Z_{L2} = j64$ Ω and $Z_{L3} = -j11$ Ω respectively. Several types of loading networks have been documented in the literature [14-18]. In this design, the proposed topology of the load network is presented in Figure 12.

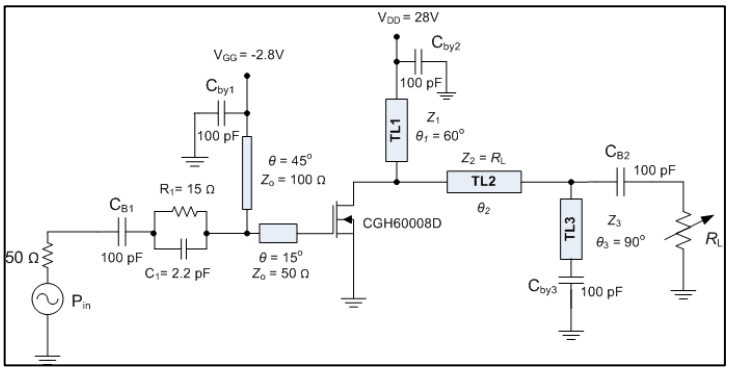


Figure 9: Schematic diagram for the circuit used to evaluate the optimum load-line resistance

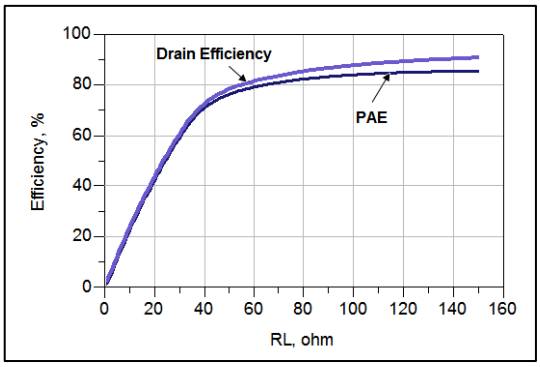


Figure 10: Variation of efficiency versus R_L

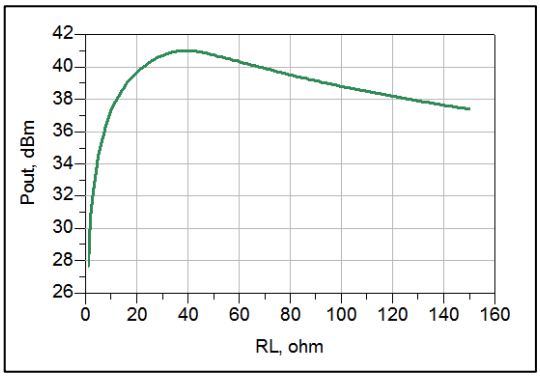


Figure 11: Simulated output power versus R_L

In this matching circuit, TL1 and TL2 are utilized to set the second harmonic impedance Z_{L2}, while TL3 and TL4 are responsible to provide the desired third harmonic impedance, Z_{L3}. On the other hand, TL5 and TL6 represent the matching elements that provide the optimum load impedance, Z_{L1}, at the fundamental frequency.

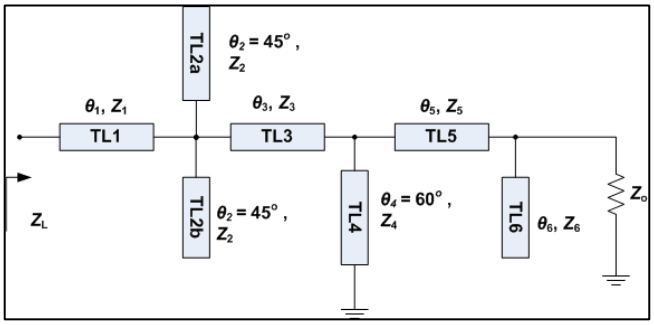


Figure 12: The suggested loading network topology for the inverse class-F power amplifier

The two parallel stubs, TL2a and TL2b, are equivalent to a single parallel $\lambda/4$ short-circuited stub and therefore they present a short circuit for the second harmonic frequency [19]. So, the resulting load network for the second harmonic is greatly simplified and is depicted in Figure 13.

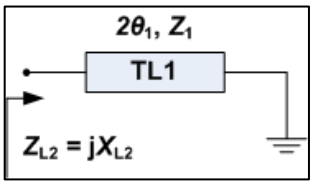


Figure 13: Equivalent load circuit at $2f_0$

Hence, the series transmission line, TL1, should provide an inductive reactance equals to X_{L2} at the second harmonic frequency and therefore its electric length θ_1 is calculated from:

$$\theta_1 = \frac{1}{2}\tan^{-1}\left(\frac{X_{L2}}{Z_1}\right) \tag{14}$$

If Z_1 is selected to be 30 Ω, then $\theta_1 = 32.44^o$.

The simplified load network at the third-harmonic component is presented in Figure 14. Since Z_1 and θ_1 are determined from the second harmonic load impedance, θ_3 and Z_3 are to be evaluated from Z_{L3}.

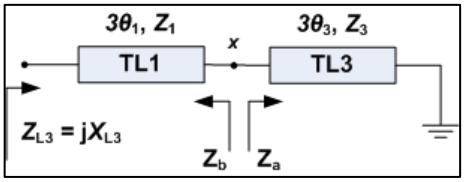


Figure 14: Equivalent load circuit at $3f_0$

The impedance Z_a, to the right of node *x* in Figure 14, is evaluated from:

$$Z_a = jZ_3 \tan(3\theta_3) \tag{15}$$

By substituting into the general transmission-line driving impedance equation, the impedance Z_b to the left of node *x* is given by:

$$Z_b = -jZ_1 \frac{X_{L3} - Z_1 \tan(3\theta_1)}{Z_1 + X_{L3} \tan(3\theta_1)} \tag{16}$$

Substituting for $Z_a = Z_b^*$ and re-arranging, the electric length of TL3 is found from:

$$\theta_3 = \frac{1}{3}\tan^{-1}\left(\frac{Z_1}{Z_3}.\frac{X_{L3} - Z_1 \tan(3\theta_1)}{Z_1 + X_{L3} \tan(3\theta_1)}\right) \tag{17}$$

If $Z_3 = 30\ \Omega$ then $\theta_3 = 20.74^o$.

The resulting loading network for the fundamental frequency is sketched in Figure 15.

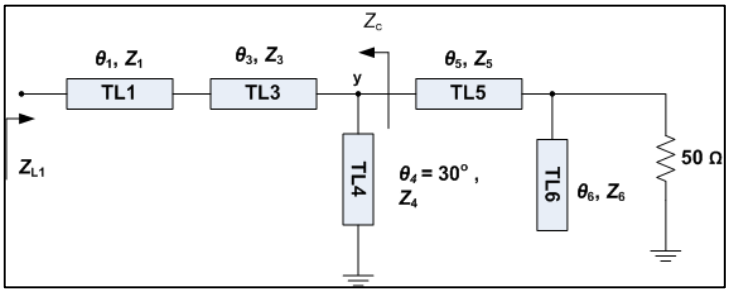


Figure 15: The equivalent loading circuit for the fundamental frequency component

The impedance Z_c seen looking into the left-side of node *y* in Figure 15 can be determined either analytically from the transmission line equations or alternatively from ADS simulation. Using the latter technique, Z_c = 12-j3 Ω. The series transmission line, TL5, and the open stub, TL6, are used to match the impedance Z_c with the 50 Ω system impedance and their electric lengths can be found graphically from the Smith chart. Accordingly, $\theta_5 = 40.8^o$ and $\theta_6 = 58.4^o$ when $Z_5 = Z_6 = 50\ \Omega$. With the output matching network connected with the drain of the GaN HEMT and the stabilization network inserted at the gate terminal, the input large signal impedance is swept versus input power and is displayed in Figure 16.

With a typical input power level of 25 dBm, the simulated input impedance is Z_{in}= 17.4-j18.6 Ω at the operating frequency. A matching circuit consisting of a series transmission line and an open-circuited stub is synthesized to match the device's input impedance with 50 Ω at 900 MHz. The completed amplifier circuit is presented in Figure 17.

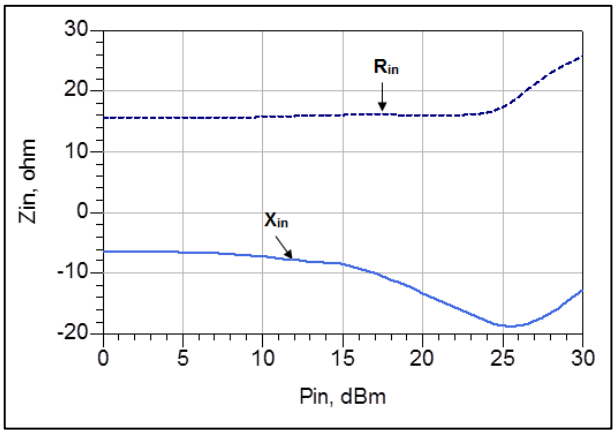


Figure 16: Variation of input large signal impedance with input power

5. Results of simulation

The power amplifier was then defined to the ADS CAD software of Keysight to test its performance using the harmonic-balance technique. In Figure 18, the drain-source voltage waveform is displayed together with its amplitude spectrum at a source power equals to 25 dBm and the operating frequency of 900 MHz. This sketch indicates that the drain signal has a half-wave rectified shape with DC, fundamental, and second-harmonic components existing at the intrinsic drain terminal of the device. The peak value of the drain voltage is about 80V which is less than the transistor's breakdown voltage.

The intrinsic drain current waveform is displayed in Figure 19 with its spectrum. Although the current waveform seems to resemble a semi-square wave, there is a considerable second harmonic component in this waveform as a result of the nonlinear behavior of the gate-source, gate-drain and drain-source capacitances of the device's model. This causes an overlap between the drain voltage and current signals and thereby increases power dissipation and reduces efficiency.

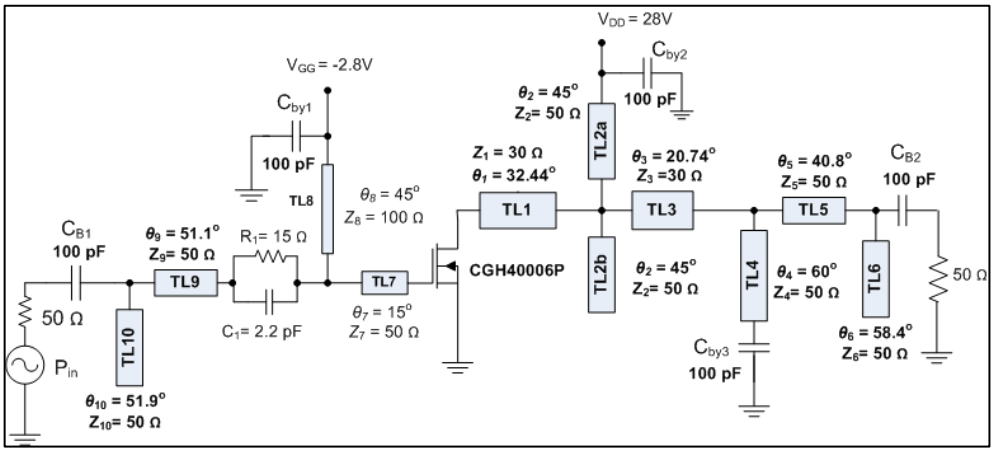
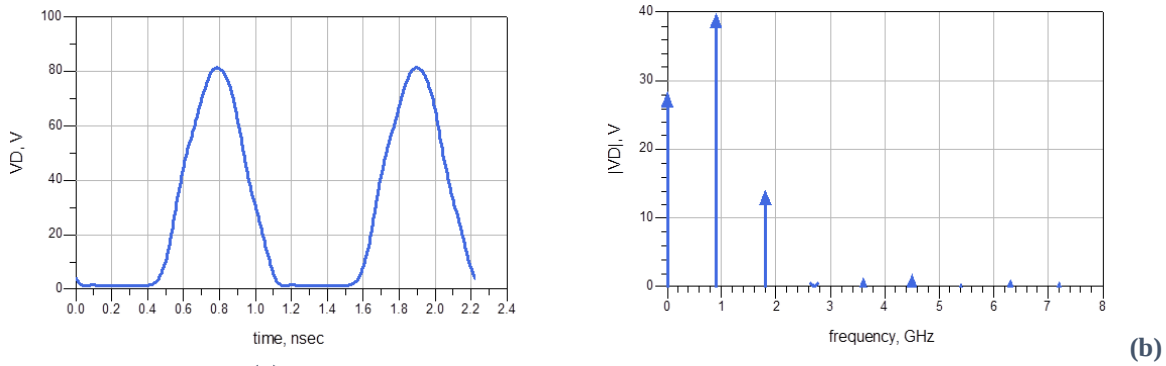
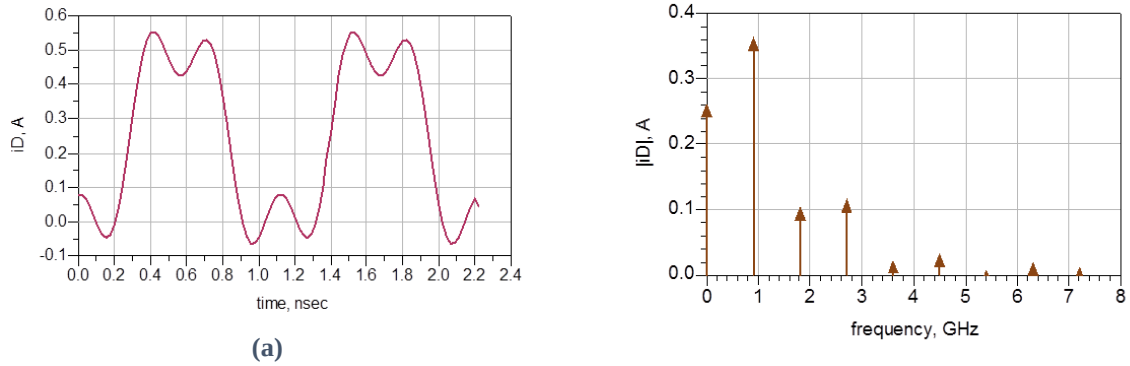


Figure 17: Schematic of the completed class-F^{-1} power amplifier circuit



(a) **(b)**

Figure 18: Intrinsic drain voltage waveform (a) and its amplitude spectrum (b)



(a) **(b)**

Figure 19: Intrinsic drain current waveform (a) and its amplitude spectrum (b)

Figure 20 presents the drain efficiency, power-added efficiency, output RF power, and power gain of the circuit versus input drive power. It seems that the drain efficiency is larger than 87% while the PAE is about 83% at source power of 25 dBm. As the input power level is increased, the power-added efficiency drops due to the roll-off in power gain beyond the 1-dB compression point. As shown from the sketch, the amplifier gives about 38 dBm RF output power when the input power is equal to 25 dBm. Beyond this input driving power level, the output is seen to be saturated at 38 dBm since the device enters deeply into saturation. The higher input power level is actually required to form the drain current signal as a semi-square wave in the inverse class-F power amplifier by raising the current third-harmonic component. The power gain of the amplifier starts compression after an input signal level of 10 dBm and reaches about 13 dB at the nominal input power of 25 dBm as depicted in Figure 20. This sketch shows also that the small signal power gain is around 20 dB.

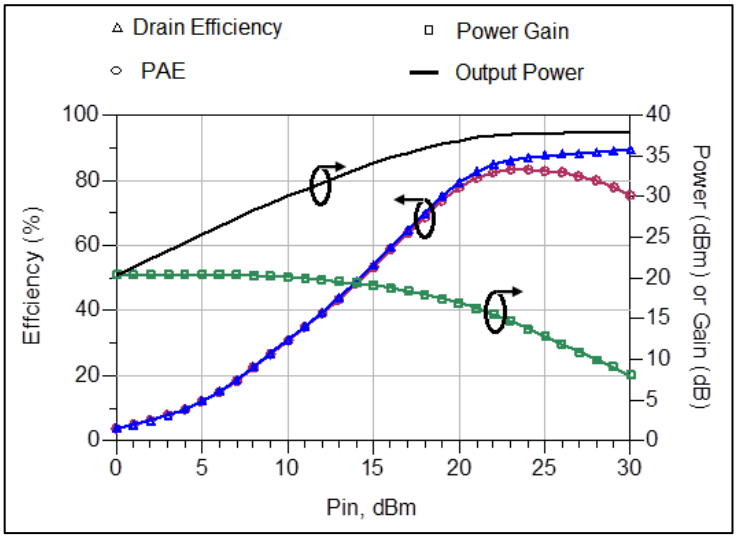


Figure 20: Efficiency, output RF power, and power gain versus input power

The drain efficiency is evaluated over a frequency band from 875 MHz to 925 MHz as shown in Figure 21 using a driving power of 25 dBm. This plot indicates that the DC-to-RF efficiency of the circuit is above 83% across the mentioned band. On the same plot, the power gain is sketched which seems to be flat over this frequency range with values around 13 ± 0.5 dB.

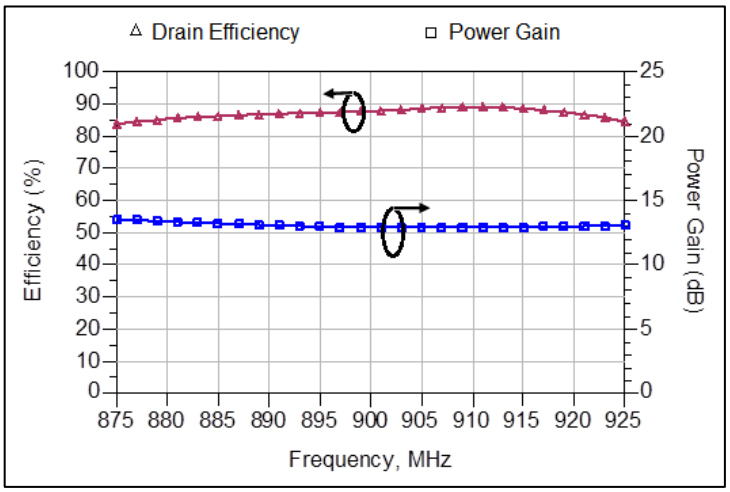


Figure 21: Drain efficiency and power gain versus frequency

The frequency response of the power amplifier circuit to a constant envelope modulated carrier, such as the GSM signal, versus offset frequency is presented in Figure 22. The spectrum is sketched around the carrier center frequency, where a data rate of 270.83 kbps and a signal bandwidth of 200 kHz are assumed. This plot shows that the signal is not greatly distorted although an input average power equals 25 dBm is used. However, the noise floor adjacent to the signal occupied bandwidth is

significantly increased which reduces the adjacent channel power ratio. Finally, Figure 23 illustrates the amplification of a variable envelope modulated carrier like the CDMA signal. This signal has a bandwidth of 1.2288 MHz with a 25 dBm average input power. The spectrum of the output signal is somewhat distorted with a degradation in the adjacent channel power ratio (ACPR). The inverse class-F power amplifier can be employed as part of the Doherty amplifier with power back-off to achieve both linearity and high efficiency when amplifying the complex modulated signals (like the OFDM-MIMO signal) in modern wireless systems [20].

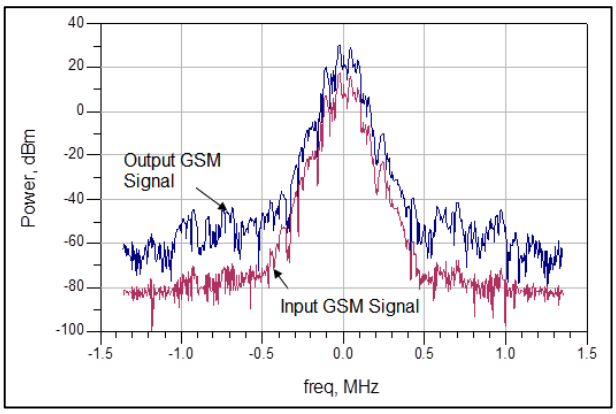


Figure 22: Spectrum of input and output GSM signals

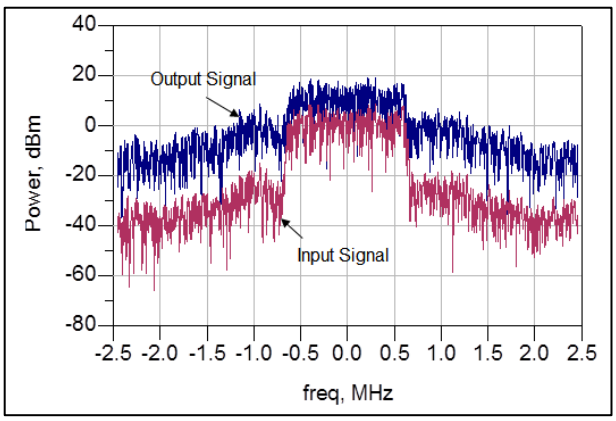


Figure 23: Spectrum of input and output CDMA signals

A comparison between the results obtained in this technique and those of some other state-of-the-art works in class-F^{-1} PA is presented in Table 1, indicating competitive performance characteristics although no optimization process has been carried out for the matching networks of the power amplifier.

Table 1: Performance comparison with other recent works

Reference	Year	Frequency (GHz)	Efficiency (%)	P_{out} (dBm)	Gain (dB)	Device Type
[14]	2011	2.14	82.4	47.6	13.6	GaN HEMT
[14]	2011	2.14	77.6	48.1	17.1	LDMOSFET
[15]	2017	2.4	87.4	44.5	11.2	GaN HEMT
[1]	2017	2.0	84.2	40.4	13.4	GaN HEMT
[7]	2018	1.227	81	54.6	12	GaN HEMT
This Work	2019	0.9	87.2	38	13	GaN HEMT

6. Conclusions

A simplified and cost-effective methodology for designing class-F^{-1} power amplifiers was presented and confirmed. This approach is dependent on extracting the optimum large-signal load impedances at the desired harmonics and based on a CAD model of the power device. Techniques for evaluating the model's internal and package elements were clarified in detail. An analytic method for synthesizing the necessary harmonic load network to realize the desired load impedances were also described in detail. A 900 MHz power amplifier circuit using a commercial 6-W GaN HEMT was designed and simulated successfully to validate the proposed approach, showing significant results that are comparable with the conventional load-pull technique. It has been verified that an appropriate analytic estimation of the optimum harmonic load impedance at the output terminals of the active device is a satisfactory replacement for the load-pull measurement setup in harmonically-tuned power amplifiers. This requires accurate modeling of the power transistor to determine the package parasitic elements and thereby to evaluate the required load impedances.

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