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Low Noise with Wide Band Transimpedance Amplifier for Nonlinear Fiber Optical Applications

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ABSTRACT

A current-mirror based transimpedance amplifier with inductor feedback simulation is reported. A 90 nm channel length process technology was simulated using N-MOSFET and P-MOSFET transistors. A transimpedance gain of 43.92 dBΩ was achieved with a bandwidth of 10 GHz (from 5 GHz to 15 GHz). The whole process was simulated using 1V DC supply voltage. From simulated data, pole frequency was found to be around 19.25 GHz. At 35 ºC, the transimpedance amplifier circuit was simulated and it was found that the input referred noise current of the circuit is 14.14 pA/√Hz at 5 GHz, 10 pA/√Hz at 10 GHz and 16.32 pA/√Hz at 15 GHz to cover the entire bandwidth of the circuit.

Keywords: Optical Preamplifier, Front-End Preamplifier, Optical receiver, Transimpedance Amplifier.

INTRODUCTION

Many challenges in Giga-bit-per-second (Gbps) fiber optic applications remain unresolved despite considerable advances in high speed electronics. The need for low power, low cost and highly efficient receiver transimpedance (TIA) devices is ever more intense. Current mirror research work is considered one of the useful tools in achieving considerable transimpedance gain. In the last year, a low power current-mirror based TIA for 10 Gbps was achieved with TIA gain of 40.5 dBΩ with f_{-3dB} bandwidth of 7 GHz and power consumption of 1.4 mW at 1V supply (Zohoori *et al*., 2018) . A 9 GHz bandwidth with 50 dBΩ TIA gain was achieved using Regulated Cascode (RGC) configuration with T-matching coil network (Seifouri *et al*., 2015). A push-pull inverter with a feedback resistor was investigated and in a later stage a coil was added in series with the feedback resistor and in this work a TIA gain of 50.8 dBΩ was reached with a bandwidth of 7.9 GHz (Salhi *et al*., 2017). An inductorless 10 Gb/s TIA using the configuration of push-pull current mirror was achieved with a TIA gain of 57.5 dBΩ and 6.6 GHz bandwidth (Hassan and Zimmermann, 2012). A transimpedance amplifier with current mirror load was investigated in which a bandwidth of 1.05 GHz with a TIA gain of 64.5 dBΩ was realized (Atef, 2014).

In this work, a highly extended TIA bandwidth is simulated using Microwave Office 2001 Software (www.ni.com) with considerable TIA gain using current mirror based transimpedance amplifier.

Transimpedance Gain Derivation:

The proposed current mirror transimpedance amplifier (TIA) circuit is shown in Figure 1. TIA gain derivation can be defined according to Mason's Rule (Mason and Zimmermann, 1960) as illustrated in Figure 2 following a Signal Flow Graph representation. This circuit topology has significant development over previous work (Phang, 2001) and (Phang and Johns, 2001) as it will be seen later. That is in addition to already reported research (Zohoori *et al*., 2018) and (Hassan and Zimmermann, 2012). As it can be seen from circuit in Fig. (1) that there is an output to input

direct feedback starting from a common-gate input configuration and ending up with a common-source output.

A current-mirror involves transistors M_2 and M_3 is biased via the output (drain) of Transistor M_1. The input current generated by the photodiode is given as I_{PD}.

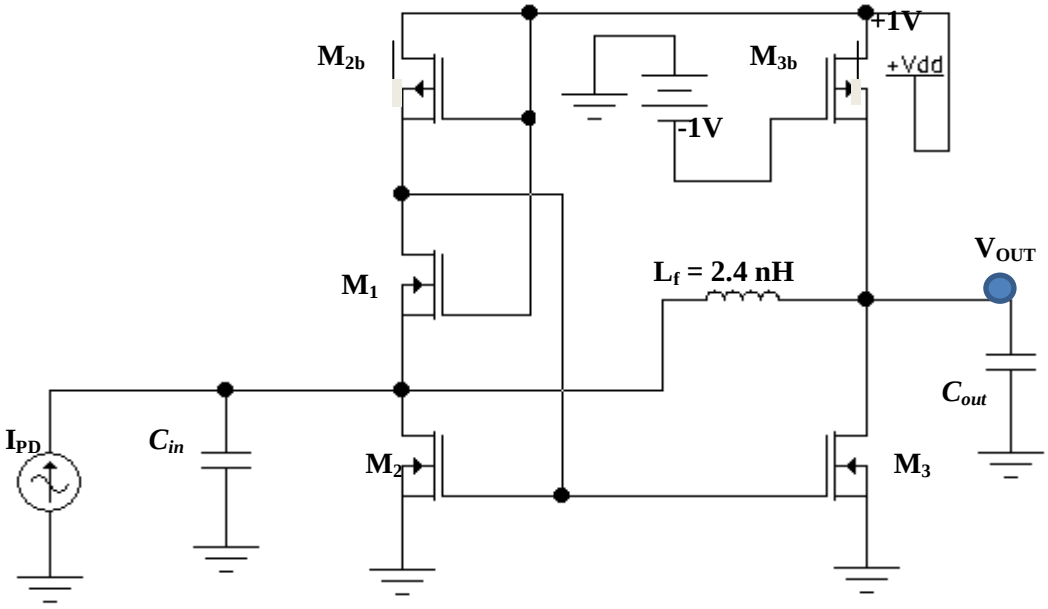

Fig. 1: The proposed transimpedance amplifier circuit.

At current gain of one, the principle of current mirror configuration is applied in which bias current at input stage is a mirror of bias current at output stage. That is because once gate-source voltage is fixed for transistors M_2 and M_3, the drain current of each transistor is considered to be a mirror for the other transistor drain current.

The general formula for the transimpedance gain follows the Mason's rule (Mason and Zimmermann , 1960):

$$\left|\frac{V_{out}}{i_{in}}(s)\right| = \frac{P_1\Delta_1}{\Delta} \qquad (1)$$

In the proposed TIA circuit and according to signal flow graph in Fig. (2), $\Delta_1 = 1$ and that is due to the fact that there is no feedback loop (*i.e.* loops L_1 , L_2 and L_3 are not touching the k_{th} forward signal path). However, $\Delta = 1 - (L_1 + L_2 + L_3)$ in which there is no sum of loops products, but only summation of individual loops subtracted from one. Therefore, Equation (1) becomes:

$$\left|\frac{V_{out}}{i_{in}}(s)\right| = \frac{P_1}{1-(L_1+L_2+L_3)} \qquad (2)$$

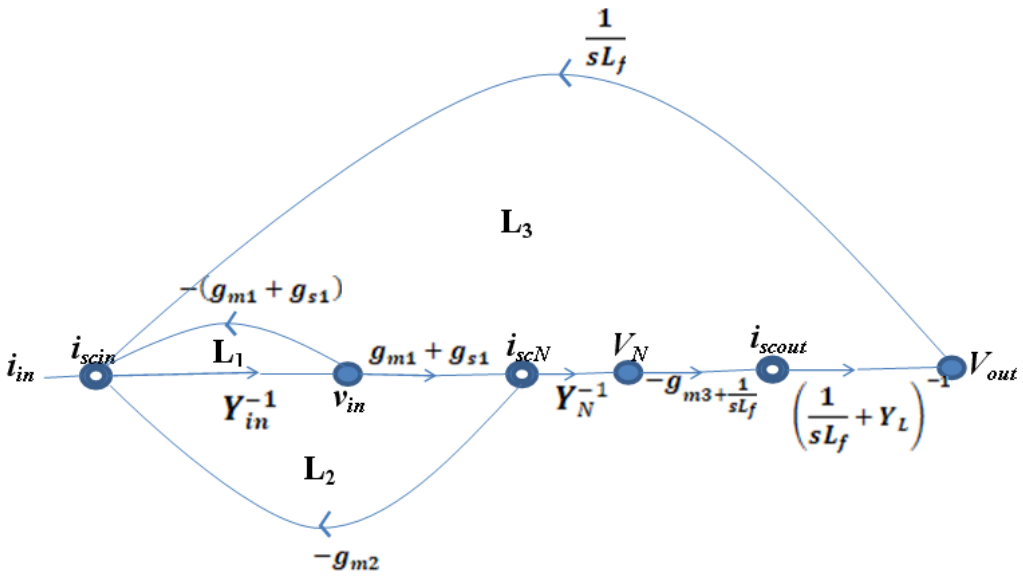

Fig. 2: Signal Flow Graph representation of the proposed TIA model

Working out P_1 as the k_{th} forward path of signal transmission as in Equation 3 and according to Fig.(2). Indicating $s = j\omega$ which follows Laplace transformation:

$$P_1 = \frac{-g_{m3}(g_{m1}+g_{s1})}{Y_{in}Y_N\left(\frac{1}{sL_f}+Y_L\right)} \quad (3)$$

Considering that g_{m3} is the transconductance of transistor M_3 , g_{m1} is the transconductance of transistor M_1 and g_{s1} is the conductance of the source at transistor M_1. Y_{in} is the input admittance of the proposed TIA circuit and is expressed as:

$Y_{in} = sC_{in}$ for which:

$$C_{in} = C_{PD} + C_{gs1} + C_{db2} \quad (4)$$

C_{PD} is the photodiode capacitance, C_{gs1} is the gate-source capacitance of transistor M_1 and C_{db2} is the drain-bulk capacitance of transistor M_2, for which C_{in} is the circuit input capacitance.

The admittance of node N is expressed as $Y_N = sC_N$ in which:

$$C_N = C_{db2} + C_{db1} + C_{gs2} + C_{gs3} \quad (5)$$

C_{db1} is the drain-bulk capacitance of transistor M_1, C_{gs2} is the gate-source capacitance of transistor M_2 and C_{gs3} is the gate-source capacitance of transistor M_3. L_f is the feedback coil inductance which was taken equals to 2.4 nH. The term sL_f represents the feedback inductive reactance and therefore, the term $\frac{1}{sL_f}$ is the feedback system frequency dependent admittance.

Loops equations are given according to Figure 2 as follows:

$$L_1 = \frac{-(g_{m1}+g_{s1})}{Y_{in}} \quad (6)$$

$$L_2 = \frac{-g_{m2}(g_{m1}+g_{s1})}{Y_{in}Y_N} \quad (7)$$

$$L_3 = \frac{-g_{m3}\left(1/sL_f\right)}{Y_{in}Y_N\left(\frac{1}{sL_f}+Y_L\right)} \quad (8)$$

By substituting Equations (3), (6), (7) and (8) in equation (1), the TIA gain is derived as:

$$\left|\frac{V_{out}}{i_{in}}(s)\right| = \left|\frac{-g_{m3}sL_f}{a_4s^4+a_3s^3+a_2s^2+a_1s+a_0}\right| \quad (9)$$

A pole zero can be found by equating the numerator $-g_{m3}sL_f$ to zero, in which $s = 0$. In Equation (9), i_{in} corresponds to I_{PD} of proposed TIA circuit in Fig.(1). The denominator root coefficients are expressed as:

$$a_4 = \frac{C_{in}C_NC_LL_f}{(g_{m1}+g_{s1})} \quad (10)$$

$$a_3 = C_NC_LL_f \quad (11)$$

$$a_2 = \left(\frac{C_{in}C_N}{(g_{m1}+g_{s1})}(1+g_{m3}) + g_{m2}L_fC_L\right) \quad (12)$$

$$a_1 = C_N \quad (13)$$

$$a_0 = g_{m2} \quad (14)$$

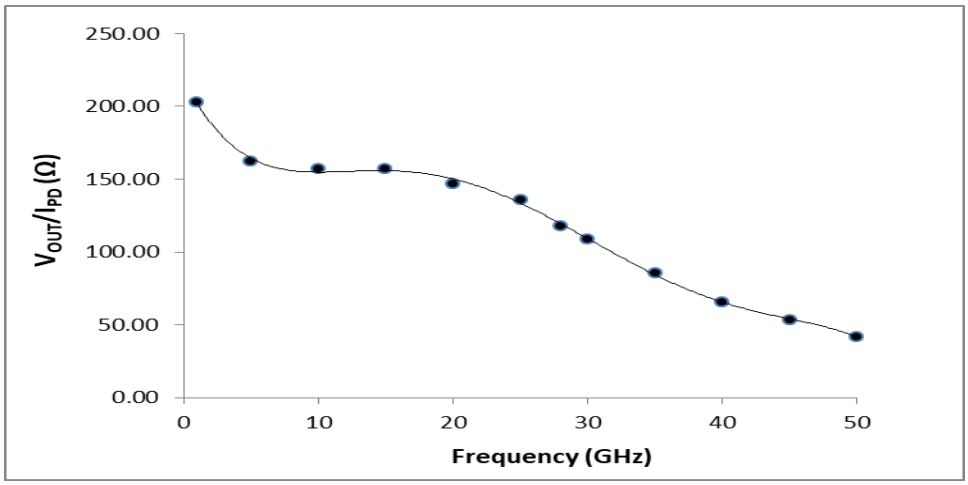

Fig. 3: Transimpedance gain simulated as V_{OUT}/I_{PD} versus frequency of the proposed circuit with 4th order fitting indicated.

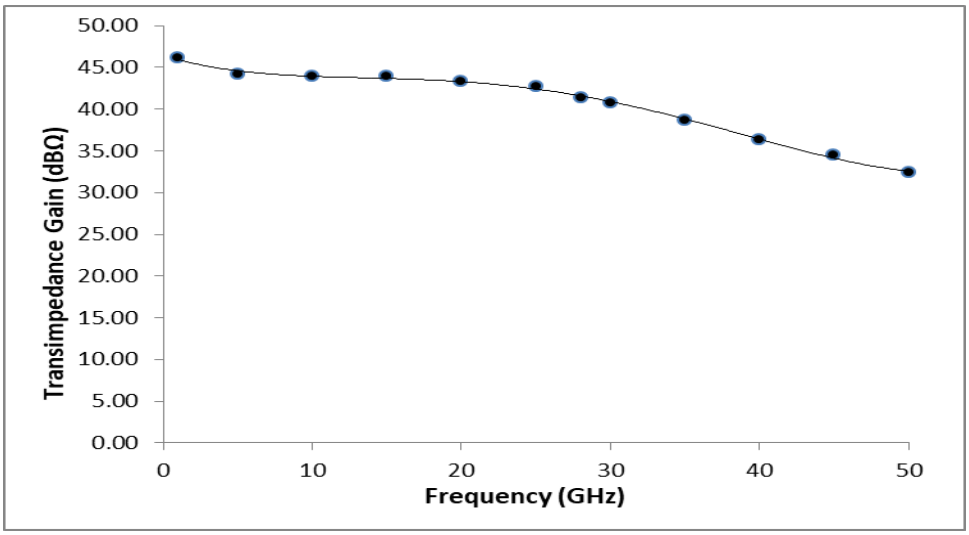

Fig. 4: Simulated transimpedance gain in (dBΩ) versus frequency of the proposed circuit with 4th order fitting indicated.

It is clear from Equation (9) and the subsequent Equations (10 – 14) that the TIA gain depends in proportional relationship on $(g_{m1} + g_{s1})$, while it is inversely proportional with all capacitances in Equations (10 -13) and that includes the most important parasitic capacitance C_{in}. Reducing circuit input capacitance C_{in} might be a great technical challenge and so as other capacitances. However, raising transconductance g_{m1} may be a good way for further improvement of TIA gain, although it may well be at the expense of circuit bandwidth for what is called a trade-off relationship between gain and bandwidth.

Simulated TIA gain of circuit proposed is shown in Fig. (3). It exhibits a transimpedance gain of around 150, meaning that V_{OUT} is 150 times I_{PD}. That is within the bandwidth of 10 GHz (between 5 – 15 GHz).

Given that input current I_{PD} is simulated at 100 µA, the output voltage V_{OUT} was obtained to be 15 mV. The general formula of Equation (9) may differ in results between different process technologies. Present research work is based on 90 nm process in which the N-MOSFET transistors M_1, M_2, M_3 are configured for an "Aspect Ratio" (W/L) of (5µm/90nm), while P-MOSFET current source transistor M_{2b} is configured for (0.9µm/90nm) and P-MOSFET current source transistor M_{3b} is configured the same as the N-MOSFET transistors. The transimpedance gain direct simulation values are taken from the simulated measurement of V_{OUT} divided by I_{PD} as in Fig.(3).

A transformation of TIA gain can be achieved in dBΩ units by taking 20 log (V_{OUT}/I_{PD}) of data in Fig. (3) to be in line with standard research work. A transimpedance gain of 43.92 dBΩ is obtained within the near flat bandwidth (BW) between 5 GHz to 15 GHz as in Fig.(4).

It was found that a near flat bandwidth (*BW*) of 10 GHz between (5 GHz to 15 GHz) according to simulated data of Figure 4. The fourth order polynomial fitting of Figure 4 suggests that the fourth order polynomial terms of Equation (9) are in good agreement with simulated transimpedance gain. A pole frequency (f_o) of 19.25 GHz is achieved indicating the endpoint of the bandwidth within the frequency response of Fig. (4).

Output Impedance:

A small signal model from the output point of view for the proposed circuit is illustrated in Fig. (5). By placing an *ac* source named V_x at the output with current named i_x then the output impedance R_{out} (frequency dependent) can be established. For the purpose of this calculation, input sources are short circuited according to Thevenin Theorem.

From the small signal analysis of Fig. (5) and by using Kirchhoff's Current Law (KCL), it is obtained that:

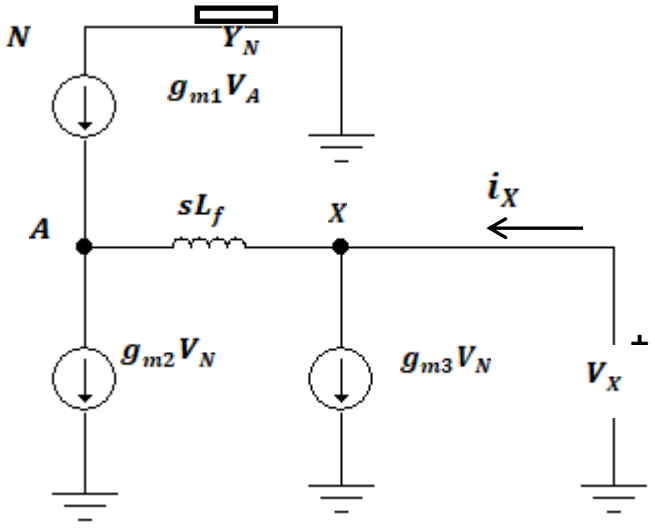

Fig. 5: Small signal model for output impedance derivation.

$$\frac{V_x - V_A}{R_f} = i_x - V_N \quad (15)$$

while from opposite direction:

$$\frac{V_A - V_x}{R_f} = -g_{m2}V_N \quad (16)$$

and therefore

$$i_x = g_{m2}V_N + g_{m3}V_N \quad (17)$$

when $V_A = 0$ (virtual ground),

$$\frac{V_x}{sL_f} = i_x - g_{m3}V_N \quad (18)$$

$$\frac{V_x}{sL_f} = g_{m2}V_N \quad (19)$$

then,

$$V_x = sL_f g_{m3} V_N \quad (20)$$

By dividing V_x by i_x, the output impedance of the proposed circuit in Fig. (1) is derived as:

$$R_{out} = \frac{V_x}{i_x} = \frac{sL_f g_{m2} V_N}{g_{m2}V_N + g_{m3}V_N} = \frac{sL_f g_{m2}}{g_{m2} + g_{m3}} \quad (21)$$

$$R_{out} = \frac{sL_f}{1 + \frac{g_{m3}}{g_{m2}}} \quad (22)$$

The term $\frac{g_{m3}}{g_{m2}}$ represents the current mirror gain of the circuit and it is obvious from Equation (22) that the output impedance of the circuit depends on frequency in a linear manner. Therefore, it is linearly proportional to the inductive reactance of the coil, while it is inversely proportional to current mirror gain. At low frequencies, the output impedance will reduce significantly, while at high frequencies, it looks like it will rise dramatically, however, that will also depends on the state of the current mirror gain. The importance of output impedance comes from the fact that if the

output of the TIA circuit is connected to a next stage, the output impedance must match the input impedance of the next stage.

Noise Optimization:

To optimize the TIA circuit in terms of noise, the dominant thermal noise is taken into account in which each transistor is mainly considered as a source of noise due to its temperature increase via circuit bias DC current. This optimization involves seeing each input signal as it is mixed with the thermal noise at its input in what is defined as an input-referred current noise. This kind of noise is represented at drain of transistors. At 35 ºC, the TIA circuit was run and it was found that the input referred noise current of the circuit is 14.14 pA/√Hz at 5 GHz, 10 pA/√Hz at 10 GHz and 16.32 pA/√Hz at 15 GHz to cover the entire bandwidth of the circuit.

The above statement is in agreement with the concept that thermal noise should cover the entire bandwidth (*i.e*. per unit bandwidth) (Razavi, 2012). Following on the TIA circuit of Fig. (1), the drain of transistor M_1 is considered the main thermal noise point as it is connected with the gate of current mirror transistors M_2 and M_3 for which the thermal noise will appear at their drains. Given the fact that the drain of transistor M_3 is connected with the circuit output, therefore, a portion of that noise will be fed back through coil L_f back to the input which is the point as the drain of transistor M_2. Hence, the terminology of input referred noise meaning that the thermal noise is missed with the main signal. Fig. (6) illustrates the input referred current noise.

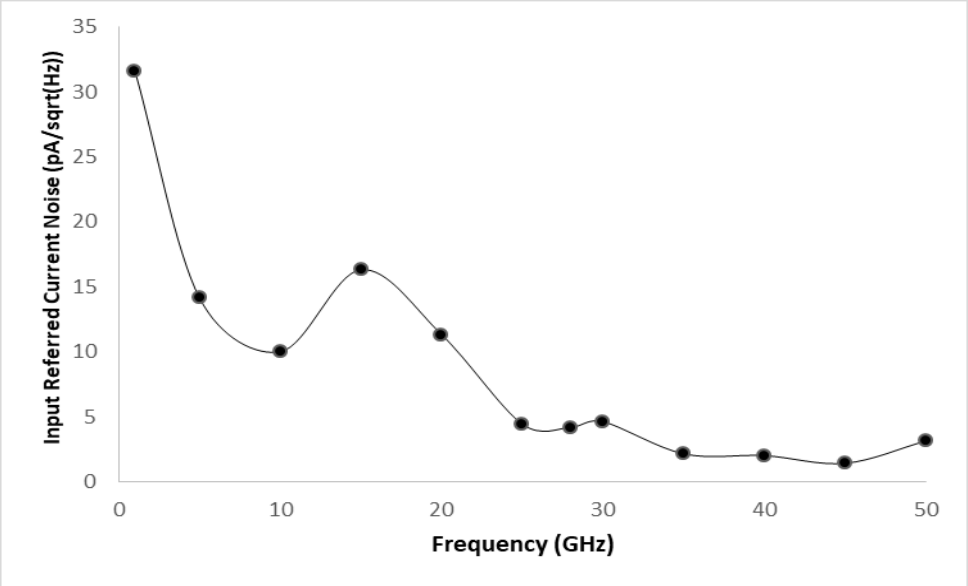

Fig. 6: Input referred noise current versus frequency of input signal

CONCLUSION

A comprehensive simulation of current-mirror based transimpedance amplifier has been achieved. The feedback system simulation resulted in a transimpedance gain of 43.92 dBΩ for a flat bandwidth of 10 GHz within the range of (5 GHz – 10 GHz). A pole frequency of 19.25 GHz showed the endpoint of the bandwidth flat response. The purpose of this work was to achieve a considerable TIA gain at maximum flat bandwidth, however, a low input referred noise current was reached for which 14.14 pA/√Hz at 5 GHz, 10 pA/√Hz at 10 GHz and 16.32 pA/√Hz at 15 GHz to cover the entire bandwidth of the circuit.

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مكبر الممانعة البينية ذو الضوضاء المنخفضة والحزمة العريضة في تطبيقات الالياف البصرية اللاخطية

الملخص

تمت النمذجة الحاسوبية لمكبر الممانعة البينية المصمم من خلال مراة التيار مع ملف حث تغذية الاسترجاع. تم استخدام نمذجة تقنية طول القناة 90 نانوميتر لترانزستورات موسفيت نوع N ونوع P. تم الحصول على ربح مكبر الممانعة البينية بمقدار 43.93 ديسبل اوم مع عرض حزمة قدره 10 كيكا هرتز (من 5 كيكا هرتز الى 15 كيكا هرتز). مجمل عملية النمذجة تمت باستخدام مصدر فولتية مستمرة مقدارها 1 فولت. تم ايجاد تردد القطب من نمذجة المعلمات والذي كان بحدود 19.25 كيكا هرتز. تمت نمذجة دائرة مكبر الممانعة البينية عند درجة حرارة 35 (سيليسيز) وقد وجد بأن تيار ضوضاء مرجعية الدخل للدائرة هو 14.14 بيكو امبير لكل جذر هرتز عند تردد 5 كيكا هرتز و 10 بيكو امبير لكل جذر هرتز عند تردد 10 كيكا هرتز و 16.32 بيكو امبير لكل جذر هرتز عند تردد 15 كيكا هرتز ليغطي مجمل عرض حزمة الدائرة.

الكلمات الدالة: المكبر الابتدائي البصري، مكبر ابتدائي نهاية – واجهة، مستلم بصري، مكبر الممانعة البينية.