Kirkuk University Journal /Scientific Studies (KUJSS)
Volume 10, Issue 3, September 2015 , p.p(79-91)
ISSN 1992 – 0849

FPGA Implementation of Mean – Max Membership based Defuzzifier Unit

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Received date: 16 / 11 / 2014 **Accepted date: 8 / 3 / 2015**

ABSTRACT

The output of fuzzification process, a fuzzy data, is unsuitable for real time applications and needs to be converted into a crisp value. The process of defuzzification is very important and has a significant impact on the overall performance of a fuzzy inference system. This paper proposes a VLSI architecture of a mean max membership (MMM) defuzzification method. The MMM of defuzzification is simple and is being generally used in comparison to more complex centre of gravity defuzzification method. The proposed architecture is modeled in very high speed hardware description language (VHDL) and implemented in Vertex-4 field programmable gate array (FPGA). The functional analysis has revealed that the proposed architecture is implementing MMM based defuzzifier accurately.

Keywords: *Defuzzification; Fuzzy processor; Mean-Max Membrtship; VLSI design.*

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تنفيذ FPGA لمعدل اعظم عضوية اعتماداً على وحدة فك الضبابية

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تاريخ استلام البحث: 16 / 11 / 2014 تاريخ قبول البحث: 8 /3/ 2015

الملخص

الناتج من عملية الغموض، بيانات غامضة، غير مناسب للتطبيقات في الوقت الحقيقي، وتحتاج إلى تحويلها إلى قيمة واضحة. عملية فك الغموض مهمة جدا ولها تأثير كبير على الأداء العام للنظام. ويقترح هذا البحث بنية معمارية من (mean max membership). وهذا الطريقة بسيطة ويتم استخدامه عادة لطرق اكثر تعقيداً من الطريقة الجاذبية (centre of gravity).في البحث المقترح تم استخدام الموديل (VHDL) لتحليل الدائرة وتنفيذها على [FPGA – (vertex – 4)]. وقد كشف التحليل الوظيفي أن الطريقة المقترحة تعتمد على الدقة.

الكلمات الدالة: فك الضبابية ؛ عمليات الضبابية ؛ معدل اعظم عضوية ؛ تصميم VLSI.

1.INTRODUCTION

The modern concept of fuzzy sets was introduced by Lotfi Zadeh [1-2] in his work "Fuzzy Sets" which described the mathematics of fuzzy set theory nearly three decades ago. Although a relatively new theory, fuzzy logic has been used in many engineering applications because being considered as a simplistic solution available for the specific problems. Fuzzy systems have high potential to understand the systems that are devoid of analytic formulations: complex systems [3-4].

Fuzzification, defuzzification and inference are three important segments of a fuzzy system. However, the fuzzy results generated cannot be used as such to the real time applications, hence it is necessary to convert the fuzzy quantities to crisp for further

Kirkuk University Journal /Scientific Studies (KUJSS)
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processing. This can be achieved by using defuzzification process. The defuzzification has the capability to reduce a fuzzy quantity to a crisp single-valued quantity. Defuzzification can also be called as "rounding off" method. Defuzzification reduces the collection of membership function values in to a single sealer quantity [5-9]. The various fuzzy systems are realized by different researcher for different applications. The original digital realization of fuzzy inference processor was performed by Toga and Watanabe [10-11]. H. Peyravi9+ et al. [12] have proposed reconfigurable inference engine for the analog fuzzy logic controller, based on Mamdani inference technique. J.M. Jou et al. [13], R. d 'Amore [14] and N. E. Evmorfopoulong et al. [15] have proposed different architecture for the fuzzy inference processor. A significant improvement is reducing power and reducing redundancy has been obtained in these structures. The inference engine performance is an important issue which needs to be addressed. Many researchers have done a work on the defuzzification fuzzy processors. Roberto d'Amore et al [12] has developed a two input one output bit scalable architecture for fuzzy processors.

In this work, we propose a VLSI architecture of a defuzzifier. The defuzzifier is based on (MMM), the simplest and generally used. The proposed architecture is modeled in very high speed hardware description language (VHDL) and implemented in Vertex-4 field programmable gate array (FPGA). In this work, two models have been designed to test the functionality of the proposed fuzzy processor. The defuzzified value has been obtained manually using the MMM technique initially, then the proposed architecture has computed the defuzzified values.

2.DEFUZZIFICATION PROCESS

The fuzzy data obtained from the fuzzification process is not suitable for the real time applications and have to be converted into crisp form. This process is known as defuzzification and it reduces the collection of membership function values into a single quantity. The different defuzzification methods used in literature are max-membership principle, centroid method, weighted average method, mean-max membership, centre of sums, center of largest area, first of maxima or last of maxima. These methods have their own applications, advantages and disadvantages [1-4]. The researchers have developed various architectures of defuzzifiers depending on what application the fuzzy processor or the fuzzy controller is being designed for. Figure (1) shows the block diagram of a defuzzifier circuit.

Kirkuk University Journal /Scientific Studies (KUJSS)
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ISSN 1992 – 0849

C1X1, C2X1, C1X2 and C2X2 are the fuzzy inputs to the defuzzifier, which comprises of elements and their associated membership functions.

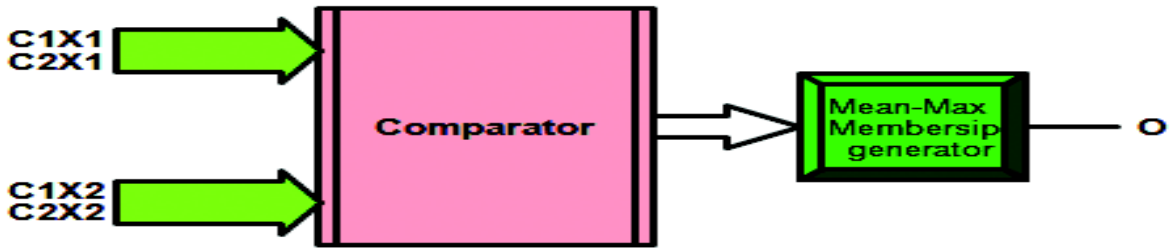

Figure (1): Block Diagram 0f a defuzzifier.

The defuzzifier block is having an architecture intact based the defuzzification techniques as mentioned above to extract the defuzzified or the crisp value. The crisp output value only can be used to control various processes or mechanisms. The defuzzification technique used in this work is the Mean – Max Membership. This method is related to max-membership principle, also is the most accurate method among all. however, in this work an accurate MMM based defuzzifier is designed and implemented. Equation 1 shows the model for the MMM based defuzzification [1-4].

$$Y_{MMM} = \frac{a+b}{2} \qquad (1)$$

Where a and b are the first and last maximum point in the x-axis of defuzzifier respectively. In this work, we have used a model to study and realize the defuzzification architecture as shown in Figure 2. In this model two rules are being fired and Mamdani implication has been used for inference. We have used aggression of rules, as the overall consequent is being obtained from the two individual consequent in each set. In each set, the minimum of two antecedent membership values is propagated to the consequent as "AND" connective is used between the two antecedents in the rule. The propagated membership value from operations on the antecedents truncates the membership function for the consequent for that rule. The truncated membership functions from each rule are aggregated according to the following equation used for conjunctive system of rules [3].

$$\mu y(y) = min\ (\mu y^{1}\ (y), \mu y^{2}\ (y), ..., \mu y^{\ r}\ (y))\ for\ y \in Y \qquad (2)$$

Kirkuk University Journal /Scientific Studies (KUJSS)
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Where uy(y) minimum of (uy^1, uy^2, … uy^r) are the principle of fuzzification

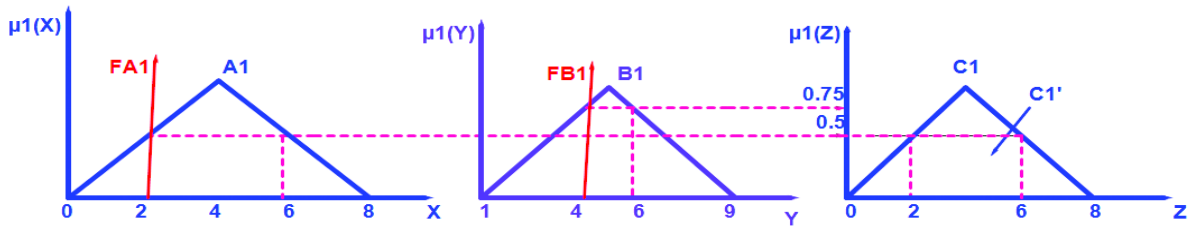
Each rule comprises of two antecedents (A1, B1 and A2, B2) and one consequent (C1, C2) an is represented as:

$$IF(X \text{ is } A1) \text{ AND } (Y \text{ is } B1) \text{ then } (Z \text{ is} C1) \quad (3)$$

$$IF(X \text{ is } A2) \text{ AND } (Y \text{ is } B2) \text{ then } (Z \text{ is} C2) \quad (4)$$

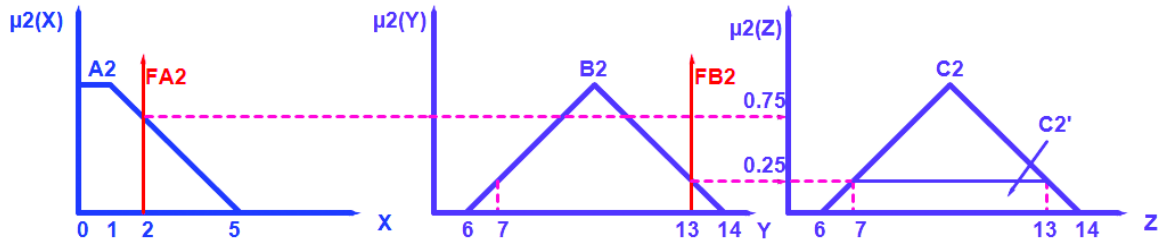
In MODEL 1, as shown in Figure (2), FA1 and FB1 are the first and second fuzzy antecedents of the first rule, respectively, and C1 refers to the fuzzy consequent of that fuzzy rule. Since; the antecedents are connected by logical "AND", therefore, the minimum membership value of the antecedents propagate through to the consequent and truncates the membership function for the consequent of each rule. Similarly, FA2 and FB2 are the first and second fuzzy antecedents of the second rule, respectively, and C2 refers to the fuzzy consequent of the second fuzzy rule. This process is the inference and it follows Mamdani's implication method, which is the most common in practice and in the literature. The union of two consequents C1 and C2 is shown in row 3 of Figure (2). From this union the defuzzified value is being obtained by using the (MMM) technique, as given in equation (1).

MODEL (1):

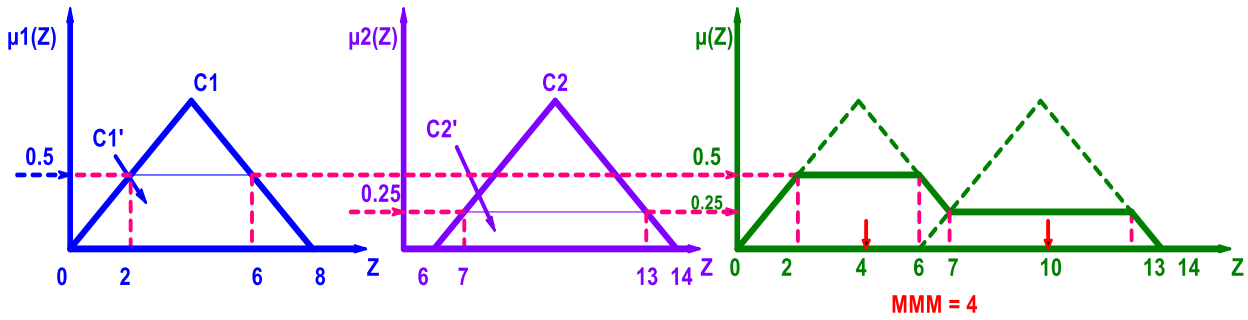


(a) :Generator C1

Kirkuk University Journal /Scientific Studies (KUJSS)
Volume 10, Issue 3, September 2015 , p.p(79-91)
ISSN 1992 – 0849



(b) :Generator C2



(c) :Union of C1 & C2

Figure (2): (a)Fuzzification, (b)Inference and (c)Defuzzification using Mean-Max Member ship for MODEL (1)

3.CALCULATION OF DEFUZZIFIED VALUES

The defuzzified or crisp value for MODEL 1 can be calculated first manually and then using the proposed architecture. It is important that the two values must match; otherwise the proposed architecture is not well designed. In this study, (MMM) is being used to calculate the defuzzified value. Figure (3) again shows the defuzzification for the MODEL 1 as given by Figure 2. The application of equation (1) to Figure 3 will generate the defuzzified value of model 1. The defuzzified value obtained out of MMM defuzzifier.

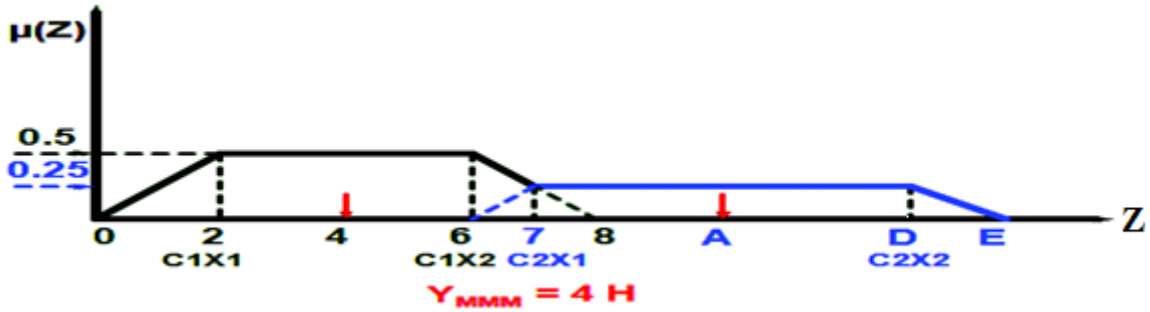


Figure (3): Defuzzification for MODEL (2)

Kirkuk University Journal /Scientific Studies (KUJSS)
Volume 10, Issue 3, September 2015 , p.p(79-91)
ISSN 1992 – 0849

Where CX1 and CX2 are the inside point of trapezoid MFs, and CX1 = a, CX2 = b

F1 = 0.5 = A H, F2 = 0.25 = 5 H, T1 = 0,

Where F1 and F2 are consequent of first rule, T1 is output of two input comparator (F1 and F2)

Hence T1 = 0 (IF F1 > F2) & T1 = 1 (IF F1 < F2)

FA1 and FB1 are the first and second fuzzy antecedents of the first rule, respectively, and C1 refers to the fuzzy consequent of that fuzzy rule.

T1 control of the output of C (C1 or C2) depends of which one of higher values point from other.

C1X1 = 2, C2X1 = 7, CX1=2,

C1X2 = 6, C2X2 = D, CX2=6,

We select C1X1 and C1X2, because; C1 is higher values point from C2, for this reason:

CX1 = 2, CX2 = 6

R3= CX1 + CX2 = 8

$$Y_{MMM} = \frac{R3}{2} = 4.$$

So the manually calculated defuzzified value is 4H. Another model of type Figure (2) has been designed and tested. The final defuzzification diagram of that model is given in Figure (4). Again MMM is used to calculate the defuzzified value. The calculations have shown that the final crisp value as AH.

Kirkuk University Journal /Scientific Studies (KUJSS)
Volume 10, Issue 3, September 2015 , p.p(79-91)
ISSN 1992 – 0849

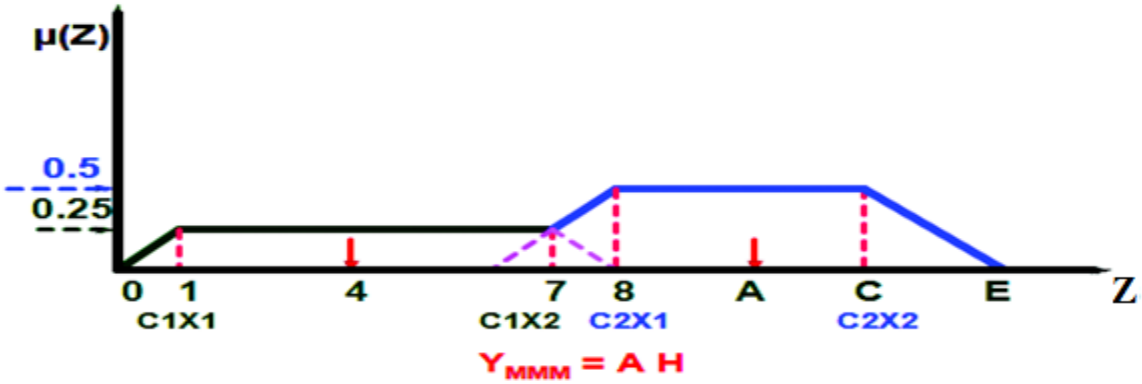


Figure (4): Defuzzification for MODEL (1)

The calculations go as follows

F1 = 0.25 = 5H, F2 = 0.5 = A H, T1 = 1,

Hence FA2 and FB2 are the first and second fuzzy antecedents of the second rule, respectively, and C2 refers to the fuzzy consequent of that fuzzy rule.

T1 = 0 (IF F1 > F2) & T1 = 1 (IF F1 < F2)

T1 control of the output of C (C1 or C2) depends of which one of higher values point from other.

C1X1 = 1, C2X1 = 8, CX1=8,

C1X2 = 7, C2X2 = C H, CX2=C H,

We select C2X1 and C2X2, because; C2 is higher values point from C1, for this reason:

CX1 = 8, CX2 = C H.

R3 = CX1 + CX2 = 20 = 14 H.

$Y_{MMM} = \frac{R3}{2} = 10 = A$ H.

The same procedure has been used for other defuzzified model, not shown in a figure. The defuzzified value obtained is 5.

Kirkuk University Journal /Scientific Studies (KUJSS)
Volume 10, Issue 3, September 2015 , p.p(79-91)
ISSN 1992 – 0849

4.HARDWARE REALIZATION OF THE DEFUZZIFICATION PROCESS

In section III, the defuzzified values have been manually calculated using the Mean–Max Membership, as shown in Figure (3) and Figure (4). However, manual calculation is not sufficient, a real hardware is needed which will automatically calculate the defuzzified values. Therefore, in this section, a novel architecture of a defuzzifier based on M. M. M. technique has been designed and simulated. The proposed architecture has been modeled in VHDL and has been implemented in field programmable gate array (FPGA). Figure (5) shows the architecture realization of the proposed architecture of equation (1). The VHDL modeling of the proposed architectures have been performed. The functional analysis is shown in Figure (6). It is clear from the functional analysis that there is a clear cut match between the results obtained manually and results generated by the architecture. In the first T-state of the functional analysis, the output of the defuzzifier 'O' is 4 H, which is same as obtained manually for Figure (3). Similarly, for T-State second and third, the outputs of the defuzzifier is AH and 5H respectively, which is same as calculated manually. This shows the proposed architecture is realizing the defuzzifier action efficiently and accurately.

5.FPGA IMPLEMENTATION OF THE DEFUZZIFIER

A Vertix-4 XC4VLX160 FPGA platform from XILINX has been used to implement the proposed architecture. The FPGA logic resource used in an implementation are shown in Table (1), schematic and of the proposed defuzzifier shown in Figure (7). The implementation results shown in Table (1) show that that there is further scope for improvement in the proposed structures by simple architecture.

Kirkuk University Journal /Scientific Studies (KUJSS)
Volume 10, Issue 3, September 2015 , p.p(79-91)
ISSN 1992 – 0849

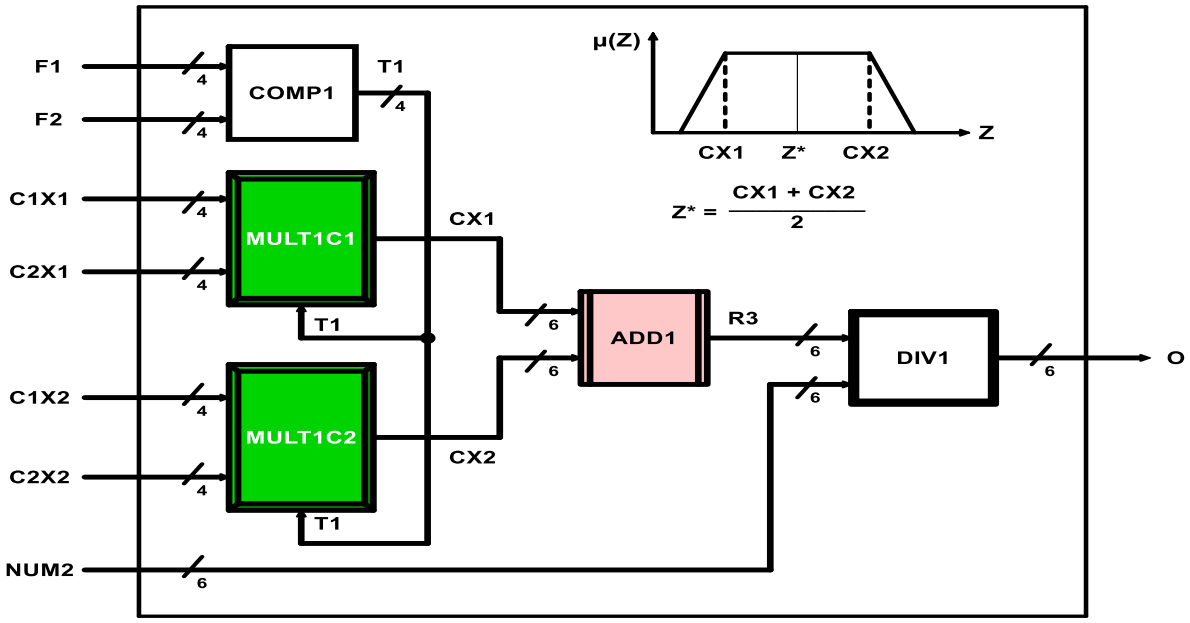


Figure (5): Proposed schematic of the defuzzifier.

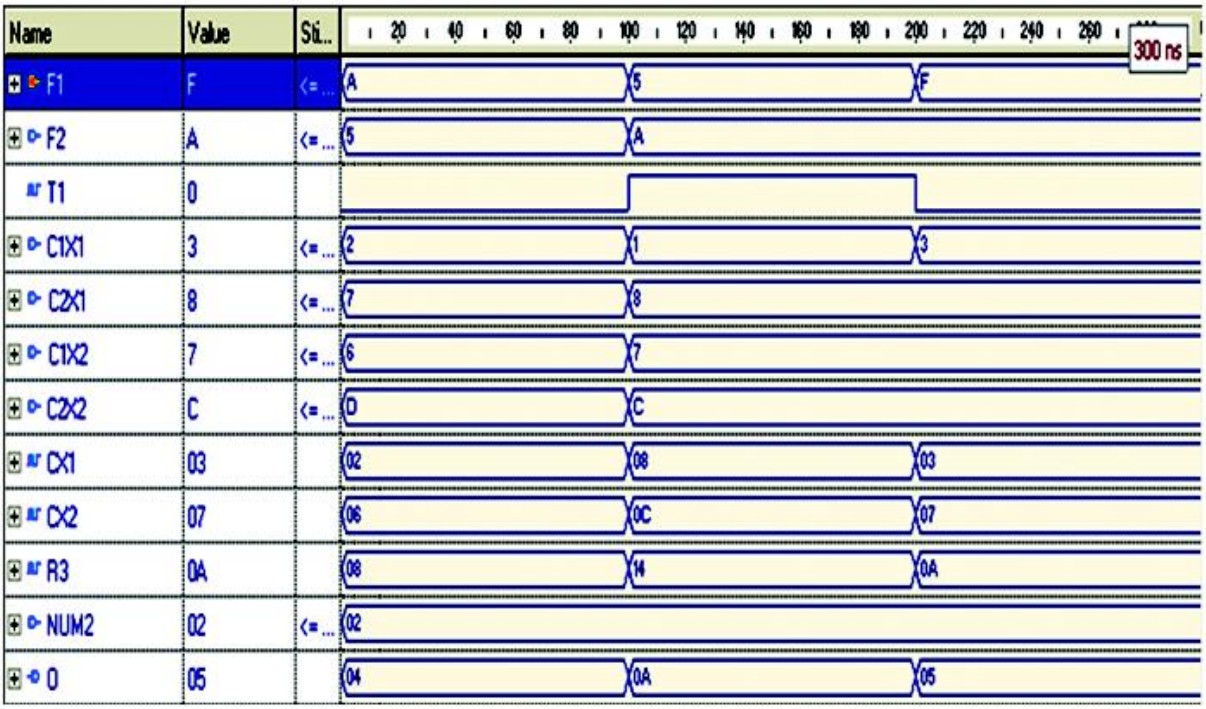


Figure (6): Timing Diagram Of The Proposed defuzzifier

Kirkuk University Journal /Scientific Studies (KUJSS)
Volume 10, Issue 3, September 2015 , p.p(79-91)
ISSN 1992 – 0849

Table (1): FPGA Implementation results

Device Utilization Summary (FPGA: XC4VLX160-FF1148)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of 4 input LUTs	142	135,168	1%
Number of occupied Slices	73	67,584	1%
Number of Slices containing only related logic	73	73	100%
Number of Slices containing unrelated logic	0	73	0%
Total Number of 4 input LUTs	142	135,168	1%
Number of bonded IOBs	36	768	4%
Average Fanout of Non-Clock Nets	3.07		

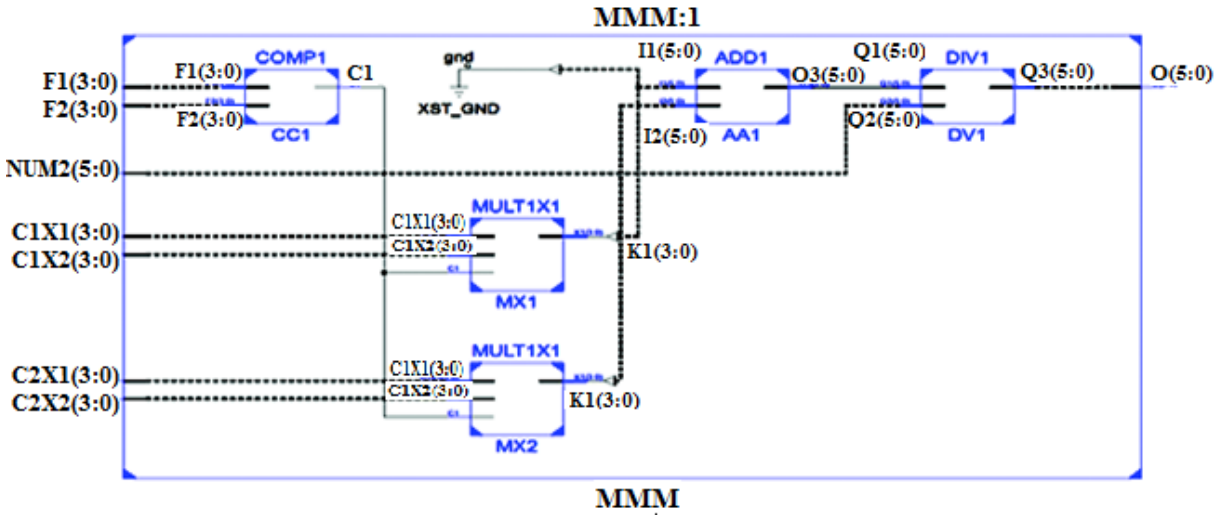


Figure (7): Schematic of the proposed defuzzifier

6.CONCLUSION

A VLSI Architecture of a defuzzifier is proposed. The proposed architecture is based on MMM. The MMM is the simplest method of the defuzzification. The defuzzified values have been initially manually calculated and finally have been obtained by the proposed architecture. The VHDL modeling and Vertex-4 FPGA implementation of the proposed architecture has been done. It has been seen that the proposed architecture realizes MMM based defuzzifier accurately, as there is a complete match between the results obtained manually and through the architecture.

Kirkuk University Journal /Scientific Studies (KUJSS)
Volume 10, Issue 3, September 2015 , p.p(79-91)
ISSN 1992 – 0849

REFERENCES

[1] L. A. Zadeh, "***Fuzzy logic***," *IEEE Computer*, vol.1 no. 4, pp. 83–93, 1988.

[2] T. J. Ross, "***fuzzy logic with engineering applications***," *John Wiley and Sons inc.*, 2005.

[3] E. H. Mamdani, "***Applications of fuzzy algorithm for simple dynamic plant***," *Proc. Inst. Elect. Eng.*, Vol. 121, pp. 1585-1588, 1974.

[4] C. C. Lee, "***Fuzzy logic in control systems: fuzzy logic controller-part I***," *IEEE Trans. Syst., Man. Cybern.*, Vol. 20, no. 2, pp. 404-418, 1990.

[5] A. M. Murshid, S. A. Loan, S. A. Abbasi, and A. M. Alamoud, "***VLSI Architecture of Fuzzy Logic Hardware Implementation: a Review***," *Int. Journal of Fuzzy Systems*, Vol. 13, No. 2, pp. 74-88, June 2011.

[6] A. M. Murshid, S. A. Loan, S. A. Abbasi, and A. M. Alamoud, "***A novel VLSI architecture for a fuzzy inference processor using Triangular-shaped membership function***," *Int.Journal of Fuzzy Systems*, Vol. 14, No. 3, pp. 345-360, Sep. 2012

[7] S. A. Loan, A. M. Murshid, S. A. Abbasi, and A. M. Alamoud, "***A novel VLSI architecture for a fuzzy inference processor using Gaussian-shaped membership function***," *Journal of Intelligent* and fuzzy systems, vol.23, pp. 1-16, 2012.

[8] Sajad A. Loan, Asim M. Murshid and Faisal Bashir, "***A Novel VLSI Architecture of a Defuzzifier Unit for a Fuzzy Inference Processor***," in proceedings of IEEE ICEASE 2013.

[9] Sajad A. Loan, Asim M. Murshid, Ahmed C. Shakir, Abdul Rahman Alamoud and Shuja A. Abbasi, "***A Novel VLSI Architecture of a Weighted Average Method based Defuzzifier Unit***," in proceedings of International MultiConference of Engineers and Computer Scientiists, Hong Kong, 12-14 March, 2014.

[10] H. Watanabe, W. D. Dettloff, and K. E. Yount, "***A VLSI fuzzy logic Controller with reconfigurable, cascade architecture***," *IEEE Journal of Solid-State Circuits*, Vol. 25, pp. 376-381, 1990.

Kirkuk University Journal /Scientific Studies (KUJSS)
Volume 10, Issue 3, September 2015 , p.p(79-91)
ISSN 1992 – 0849

[11] M. Togai and H. Watanabe, "***Expert system on a chip: an engine for real-Time approximate reasoning***," *IEEE Expert Mag.*, Vol. 1, pp. 55- 62, 1986.

[12] H. Peyravi, A. Khoei, and K. Hadidi, "***Design of an analog CMOS fuzzy logic controller chip,"*** Fuzzy Sets and Systems 132, PP. 254- 260, 2002.

[13] J. M. Jou and P. Y. Chen, "***An adaptive fuzzy logic controller: its VLSI architecture and applications***," *IEEE Trans. Very Large Scale Integration (VLSI) Systems*, Vol. 8, pp. 52-60, 2000.

[14] R. d'Amore, O. Saotome, and K. H. Kientiz, "***A Two – Input, One – Output Bit – Scalable Architecture for Fuzzy Processors***," *IEEE Computer Society press*, vol. 18, pp. 56-64, July 2001.

[15] N. E. Evmorfopoulos, and J. N. Avaritsiots, "***An adaptive digital fuzzy architecture for application-specific integrated circuits***," *Active and Passive Elec. Comp.*, Vol. 25, pp. 289-306, 2002.

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