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Design of RF Power Amplifiers using Parallel-Series Power Combining Transformers

Suhad. H. Jasim
Electrical Engineering Department, University of Technology/Baghdad.
Email: suhadhusin@yahoo.com
Dr.Ahmed S. Ezzulddin
Electrical Engineering Department, University of Technology/Baghdad.
Email: ase.uot@gmail.com

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ABSTRACT

This paper presents the design of a one watt-level RF CMOS Power Amplifier (PA) based on power combining transformers PSCT in 0.13 µm technology using ADS 2011.10. The PA incorporates a parallel combination of four differential PA cores to generate high output power with acceptable efficiency and linearity. The first part the design for class-AB PA for WLAN applications is presented. The PA delivers an Output Power (Pout) of 30 dBm, Power Gain (Gp) of 30 dB and 40% PAE using 2.5 V supply. In the second part a class-E PA is designed to provide an output power of 30 dBm, power gain of 30 dB, and 54% PAE at 2.45 GHz using 1.6 V supply. The layout of the transformers is designed and simulated with momentum RF EM simulator of ADS 2011.10 in order to realize a fully integrated power amplifier. The simulated efficiency of the designed transformer was 78% with minimum insertion losses (*ILmin*) of 0.87 dB.

تصميم مضخمات قدرة راديوية التردد بتقنية CMOS مع محولات جامعة للقدرة النوع المتوازي- المتوالي PSCT

الخلاصة

يتضمن هذا البحث تصميم ومحاكاة لاثنين من مضخمات القدرة راديوية التردد عالية الكفاءة وبمستوى قدرة يصل الى الواط مع محولات جامعة نوع PSCT باستخدام تقنية CMOS وباجراء (0.13 µm) بمساعدة حقيبة المحاكاة ADS 2011.10 مع نموذج المحاكاة BSIM4 للترانزستر MOSFET. تم في الجزء الاول تصميم مضخم قدرة من الصنف AB ويصلح للاستخدام في تطبيقات WLAN. تمكن هذا المضخم من تجهيز قدرة خرج مقدارها 30 dBm وربح قدرة 30 dB وكفاءة قدرة مضافة 40% لمجهز 2.5 V. اما في الجزء الثاني فقد تم تصميم مضخم قدرة من الصنف E . تمكن هذا المضخم من تجهيز قدرة خرج مقدارها 30 dBm وربح قدرة 30 dB وكفاءة قدرة مضافة 54% لمجهز 1.6 V. ولتحقيق مضخم القدرة المتكامل، تم تصميم التخطيط للمحول الجامع على الرقاقة نوع PSCT والمستخدم مع المضخمين المقترحين، كذلك تمت المحاكاة باستخدام طريقة الزخم

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2412-0758/University of Technology-Iraq, Baghdad, Iraq

الكهرومغناطيسي للموجات الرادوية واظهرت النتائج للمحول PSCT كفاءة مقدارها 78% وخسائر ادراج صغرى 0.87 dB.

Keywords: RF power amplifier, class-E, class-AB, CMOS technology, power combining transformer.

INTRODUCTION

CMOS has for a long time been a good choice for digital integrated circuits (IC) due to its low cost, high level of integration and constant enhancements in its performance. Due to the significant scaling of MOS transistors, the transition frequency has reached well beyond 100 GHz and CMOS technology have become popular in wireless applications. At high frequencies, the major difficulty for CMOS PA is to achieve high output power. This is because at high frequencies, CMOS has low DC bias voltage of only about 2 volts. This low DC bias voltage has two effects, first relatively low RF output power due to low DC input power for any reasonable value of DC input current, second the optimum impedance is proportional to (V_{DC}/I_{DC}). Low DC supply voltage leads to low RF impedance, which is very difficult to match to 50 ohms load impedance without losses. Furthermore, silicon substrate is usually conductive, which results in substantial additional loss at RF frequencies.

Power Combining Techniques

Transform-type combiner can be categorized as Series-Combining Transformers (SCTs) and Parallel-Combining Transformers (PCTs) according to their ways of voltage and current combining at the load. The advantage of PCT configuration is a reduction of the secondary inductor losses due to a reduction of the current flowing through them but at the cost of a larger area and a lower self-resonant frequency. Moreover, the PCT requires higher turn ratios in order to get the same output impedance compared to a SCT, which increases the losses in practice. On the other hand, a combination of SCT and PCT topologies is also possible in order to combine the advantages of both transformer topologies in a Parallel-Series Combining Transformer (PSCT) topology [1].

The hybrid-type power combining transformer (PSCT) performs the parallel (or current) and the series (or voltage) combining simultaneously in a single structure enabling the implementation of the power combining transformer in a smaller form-factor compared to the SCT. Moreover, the mutual inductance at the primary side in the PSCT is increased due to additional coupling between adjacent primary inductors, leading to improved efficiency and PTR (Power Transmission Ratio). The PSCT topology and its equivalent circuit model are presented in Figure (1).

The total combining inputs in the PSCT is M =N_P*N_S where N_P, N_S are the parallel and series combining parts respectively. the input impedance of the PSCT can be obtained by the following equations [1]:

$$Z_{IN-PSCT} = Z_{1-PSCT} + \frac{N_P}{N_S N^2}\left[\frac{1}{1+\frac{Z_{2-PSCT}N_P}{j\omega K N^2 N_S L_1}}\right] Z_{2-PSCT} \quad ...(1)$$

If the coupling effect and the frequency dependent inductor are ignored, the input impedance of the PSCT can be simplified as:

$$Z_{IN-PSCT-Ideal} = \frac{N_P}{N_S N^2} R_L \quad ...(2)$$

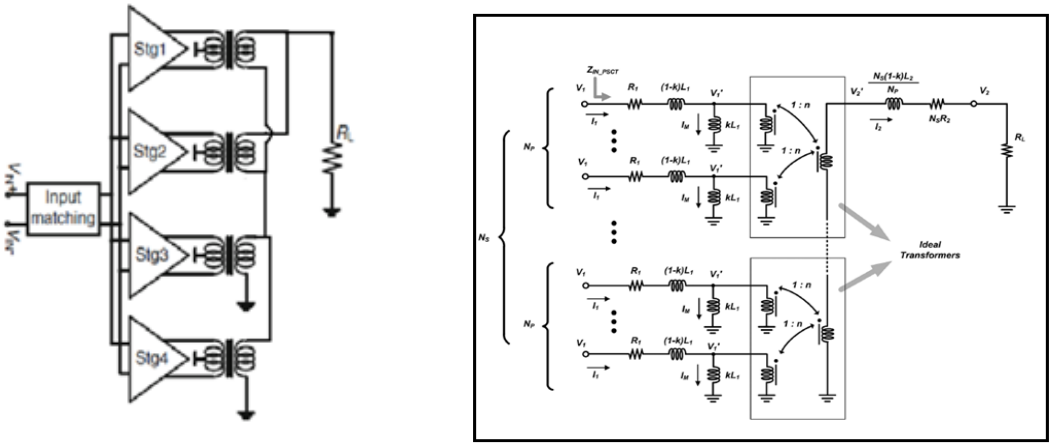
The input impedance of the PSCT is negligibly affected by the number of combining inputs if the number of series and parallel combining parts are same. The efficiency and the optimal primary inductance value of the PSCT can be obtained by the following equations [1]:

$$L_{1\_OPT\_PSCT} = \frac{R_L}{N_S N^2 \omega} \sqrt{\frac{1}{Q^2} + \frac{1}{N_P{}^2} + \frac{K^2}{N_P}} \quad ...(3)$$

$$\eta_{PSCT} = \frac{\omega L_1}{\frac{N_P N_S N^2}{Q K^2 R_L}\left(\frac{1}{Q^2}+\frac{1}{N_P{}^2}+\frac{K^2}{N_P}\right)(\omega L_1)^2+\left(\frac{2N_P}{Q^2K^2}+1\right)(\omega L_1)+\frac{N_P R_L}{N_S N^2 Q K^2}} \quad ...(4)$$

Where

N represents the turn ratio of the transformer, K is the coupling factor, and Q is the quality factor.



(a) **(b)**

Figure (1): (a) Simplified schematic of the PSCT topology, (b) The equivalent circuit model of the transformer.

Design of a Watt-Level Class AB Power Amplifier for WLAN Applications

In Class AB, the conduction angle is between 180◦ and 360◦, the DC bias voltage of the gate-to-source (V_{GS}) is slightly above the threshold voltage (V_T) and the transistor is biased at a small drain current. As the name suggests, class-AB is the intermediate class between class-A and class-B. A single-ended class-AB power amplifier topology is shown in Figure (2). For a 0.13 µm CMOS, 1.2 V and 2.5 V are available. Using

Equation (5) the deliverable output power to 50 Ω load are 14.4 mW and 62.5 mW under 1.2 V and 2.5 V respectively without any impedance transformation [2]:

$$P_{OUT} = \frac{V_{DD}^2}{2R_L} \quad ...(5)$$

$$R_{OPT} = \frac{V_{DD}^2}{2P_{MAX}} \quad ...(6)$$

Equation (6) gives the optimum load to be presented at the PA outout, Under 1.2 V and 2.5 V for an output power 125 mW are 6 Ω and 25 Ω respectively. It is clear that 1.2 V is not sufficient because impedance transformation between 6 Ω and 50 Ω is too hard to be realized in practice. So, 2.5 V is a good choice for the design. The *LC* tank circuit $(L_o,\ C_o)$ is designed to resonate at ω_o and block higher harmonics from proceeding towards the load, so that [3]:

$$X_{Co} = X_{Lo} = \frac{R_{OPT}}{Q_L} \quad ...(7)$$

$$L_o = \frac{X_L}{\omega_o} \quad ... (8)$$

$$C_o = \frac{1}{\omega_o X_C} \quad ...(9)$$

Where

Q_L is the load quality factor and is selected to be 15. Using the load pull simulation , the value of the optimum load impedance obtained from the simulation ($Z_{OPT} = 13.132 + j3.026$) at which the individual PA can deliver 25.6 dBm with maximum PAE.

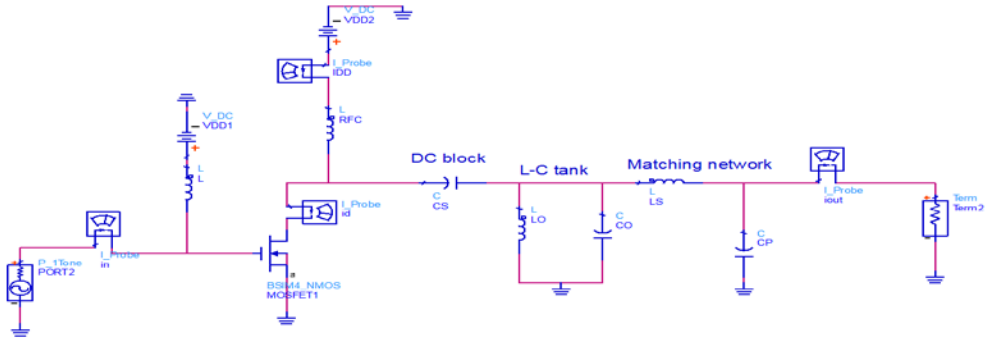


Figure (2): Schematic of a single stage class _AB power amplifier.

Class -AB Power Amplifier Design Based on PSCT

The PA is a four stages, all transformer-coupled design, the turn ratio of the transformer can be determined using Equation (4) with N_P and N_s are equal and $Z_{IN-PSCT-Ideal}$ is the optimum load impedance of the PA that is determined by the load pull simulation $|Z_{OPT} = 3.4|$, R_L is 50 Ω. The schematic and the performance of the PA are shown in Figure (3) and (4) respectively. The power amplifier delivers an output power of 30 dBm with PAE of 40% at an input signal level of 0dBm. The simulated performance of the PA as a function of frequency for an input power of 0 dBm is

shown in Figure (5). As shown from this figure, the minimum PAE is 40 % while the output power PA remains almost flat over the band which is from 2.4 GHz to 2.48 GHz . Using WLAN IEEE 802.11g transmitter test bench of ADS 2011.10, the measured spectrums and constellations for the WLAN signals are presented in Figure (6).Finally, The characteristics of the PA, compared with other recent works are summarized in Table (1).

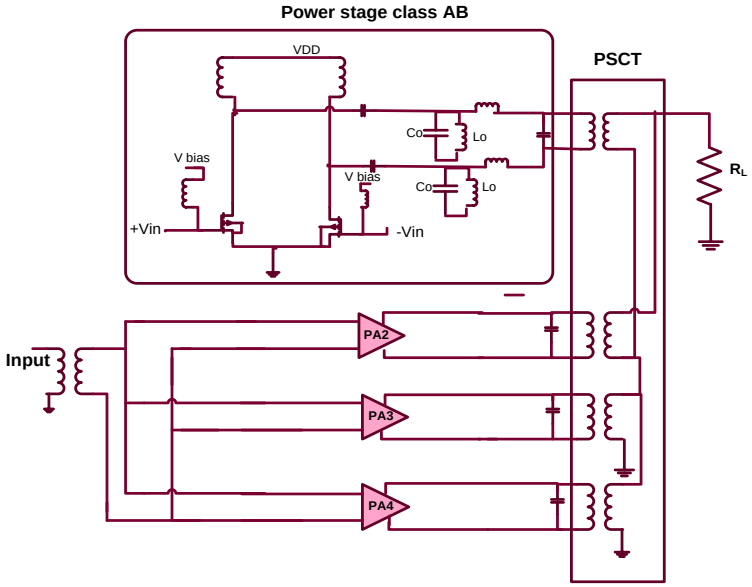


Figure (3): Schematic of the PA based on PSCT.

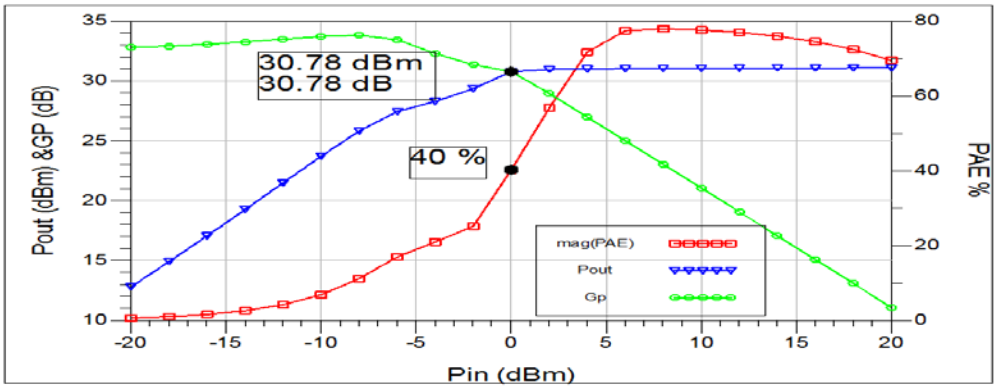


Figure (4): Simulation results of class AB PA based on PSCT.

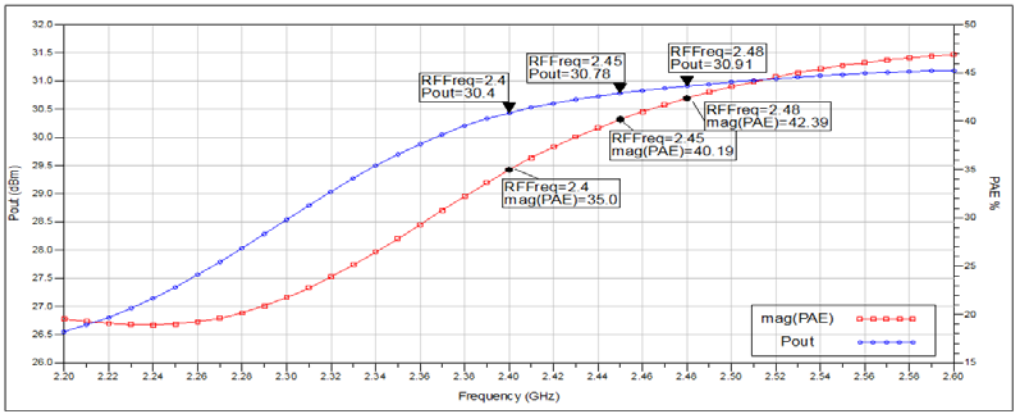


Figure (5): The performance of the PA based as a function of frequency.

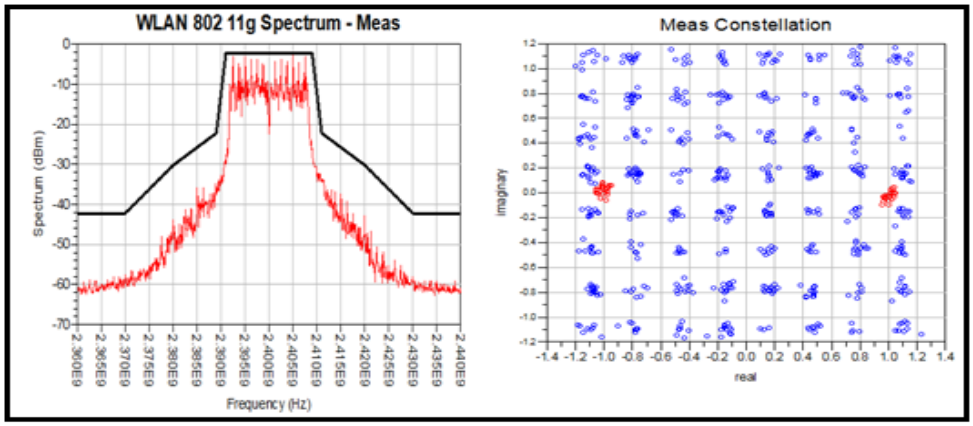


Figure (6): Spectrum and constellation for WLAN 54 Mbps 64-QAM signal.

Table (1): Performance comparison of watt-level class AB PAs.

Reference	[3]	[5]	[6]	[1]	[7]	This Work
Year	2009	2011	2012	2012	2013	2014
CMOS Technology	0.13 µm	0.18µm	0.90 nm	0.18µm	65nm	0.13
Frequency (GHz)	2.4	0.9	2.3	2.4	2.4	2.45
Pout (dBm)	30	29	30.1	23.5	33.5	30
PAE (%)	18	24	33	34.9	37.6	40
V_{DD} (V)	1.8	3.3	1	3.2	3.3	2.5
Combining technique	SCT	SCT	PCT	PSCT	PCT	PSCT

Design of a Watt Level Class-E Power Amplifier using Power-Combining Transformers

A single-ended class-E amplifier with shunt capacitor topology is shown in Figure (7). The component values of the single ended class E PA are calculated at output power 125 mW (≈ 21 dBm), operating frequency 2.45 GHz. In 0.13 μm CMOS technology drain supply voltage of 1.2 V and 2.5 V are available, both values will provide an impedance transformation ratio that is too hard to be realized in practice for the PA design based on PSCT. Therefore the supply voltage is chosen to be 1.6 V. The components values are determined using the following equations [10]:

$$R_S = \frac{8V_{DD}^2}{(\pi^2+4)P_{OUT}} \quad ...(10)$$

$$L_S = \frac{\pi(\pi^2-4)\,V_{DD}^2}{2(\pi^2+4)\,\omega_o\,P_{OUT}} \quad ...(11)$$

$$C_S = \frac{P_{OUT}}{\pi\omega_o\,V_{DD}^2} \quad ...(12)$$

$$C_{OS} = \frac{1}{\omega_o\,Q_{LS}R_S} \quad ...(13)$$

$$L_{OS} = \frac{Q_{LS}R_S}{\omega_o} \quad ...(14)$$

R_s is usually called optimum load resistance (R_{opt}) designed according to the specification on output power and the supply voltage. The series tank, consisting of L_{OS} and C_{OS} , is inserted to suppress higher harmonic content in the load.. L_{RFC} can be calculated by the resonant equation of an LC tank [8]:

$$L_{\mathrm{RFC}} = \frac{1}{\omega_o^2 C_1} = \frac{1}{\omega_o^2(c_p - c_s)} \quad ...(15)$$

where

C_1 is the cancelation capacitance by the inductor, C_p is the MOSFET output capacitance and C_s is the capacitance of the class_E PA. LC tank is the most simple and straight forward matching network that has been widely used in all kinds of PAs, however. A single-stage LC tank matching network basically has a forms as shown in Figure (8). The values of L_m, C_m, and L_{total} can be calculated using the following equations [9]:

$$L_m = \frac{\sqrt{R_{opt\,(R_L - R_{opt})}}}{\omega_o} \quad ...(16)$$

$$C_m = \frac{\sqrt{(R_L - R_{opt})/R_{opt}}}{\frac{R_L}{\omega_o}} \quad ...(17)$$

$$L_{total} = L_x + L_m \quad ...(18)$$

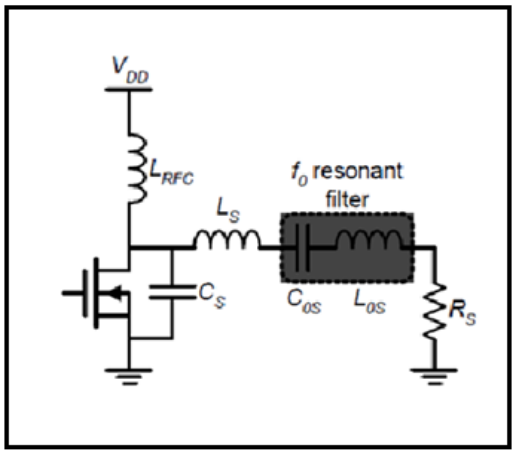


Figure (7): Single-ended class-E PA with shunt capacitor.

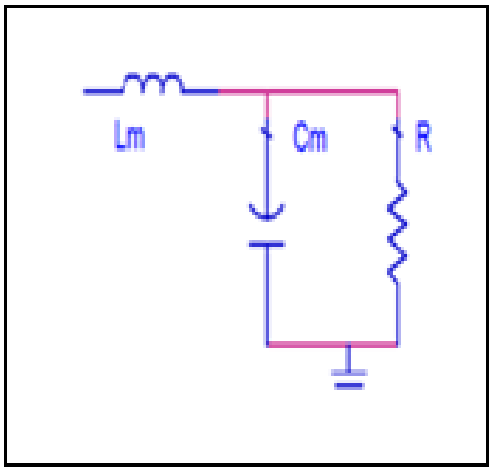


Figure (8): Single-stage L-C matching network

Class-E Power Amplifier Design Based on PSCT

The designed PA incorporates four stages differential stages with each stage delivers 250 mW approximately based on PSCT power combining. The topology of differential PA is shown in Figure(9).The schematic and the performance of the designed PA based on PSCT as a function of the input power are shown in Figure (10) and (11) respectively, it delivers an output power of 30 dBm with PAE of 54% at input power 0 dBm. In order to estimate the linearity of the PA, the 1-dB gain compression simulation is performed, the simulation result is shown in Figure (12). The power amplifier reaches its output 1-dB compression at 30 dBm, with an input power level of 1 dBm. The simulated performance of the PA as a function of frequency for an input power of 0 dBm is shown in Figure (13). As shown from this figure, the output power of the PA remains almost flat over the band, which is from 2.4 GHz to 2.48 GHz. The minimum PAE is 51.6 % . The performance of the designed PA is compared with other state-of-the-art linear CMOS PAs as illustrated in Table (2).

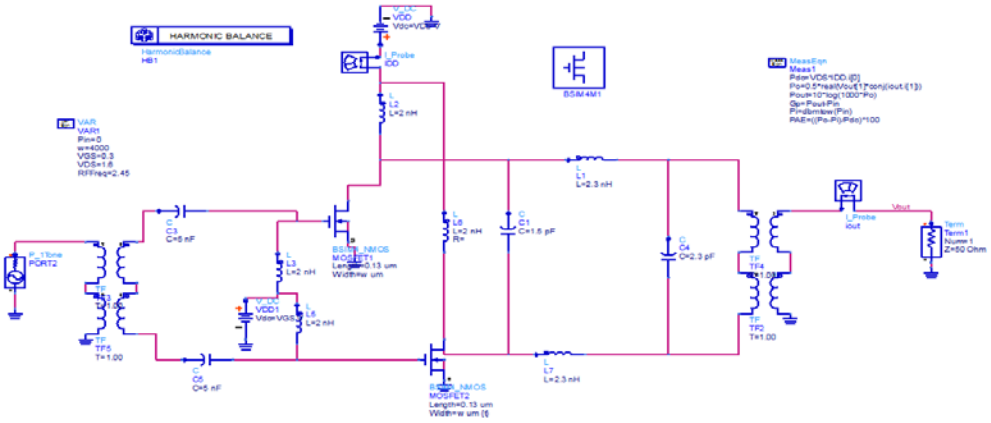


Figure (9): Schematic of differential class-E power amplifier.

Table (2): Performance comparison of watt-level class E PAs.

Reference	[10]	[11]	[12]	[13]	This Work
Year	2008	2009	2012	2013	2014
CMOS Technology	0.18 µm	0.18µm	0.18µm	0.25 µm	0.13
Frequency (GHz)	1.8	1.71	5.2	5.3	2.45
Pout (dBm)	31.2	33.4	23.4	30.3	30
PAE (%)	41	50	21	17.8	54
V_{DD} (V)	3.3	3.3	3.3	6.35	1.6
Combining technique	PCT	SCT	PCT	PSCT	PSCT

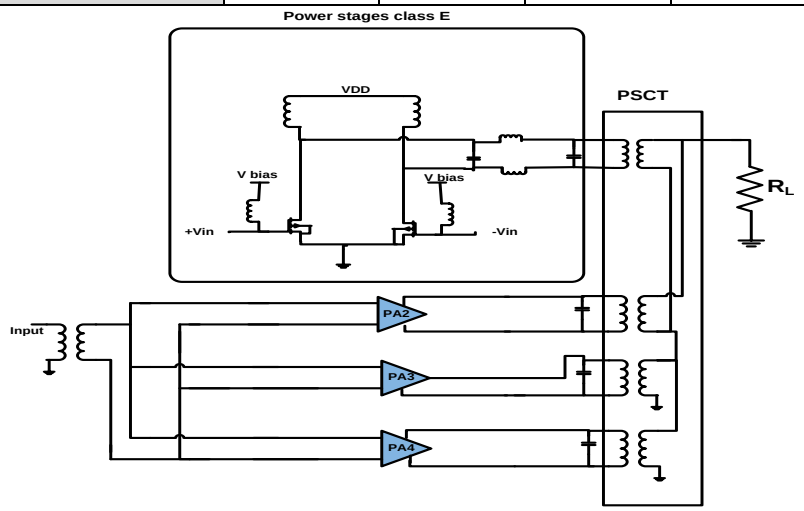


Figure (10): Schematic of the PA based on PSCT.

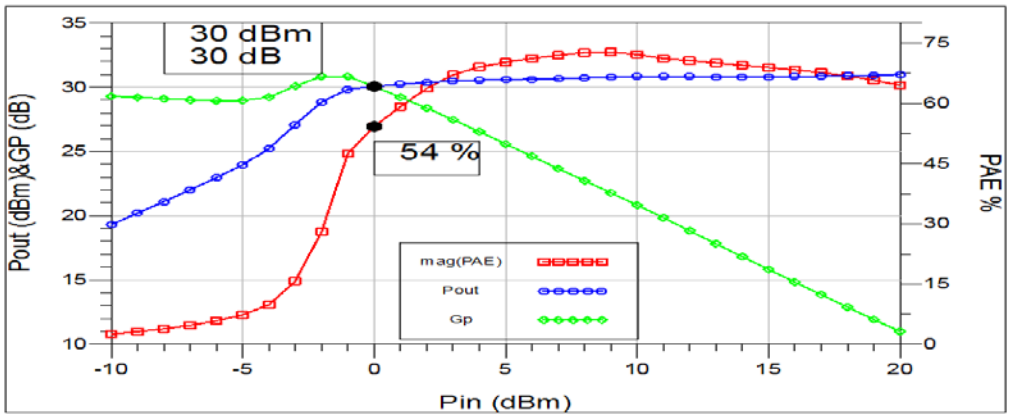


Figure (11): The performance of the PA as a function of input power.

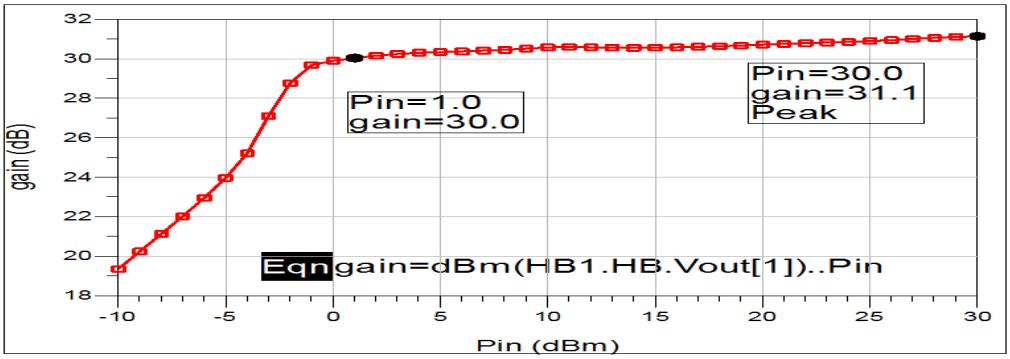


Figure (12): Gain compression simulation result.

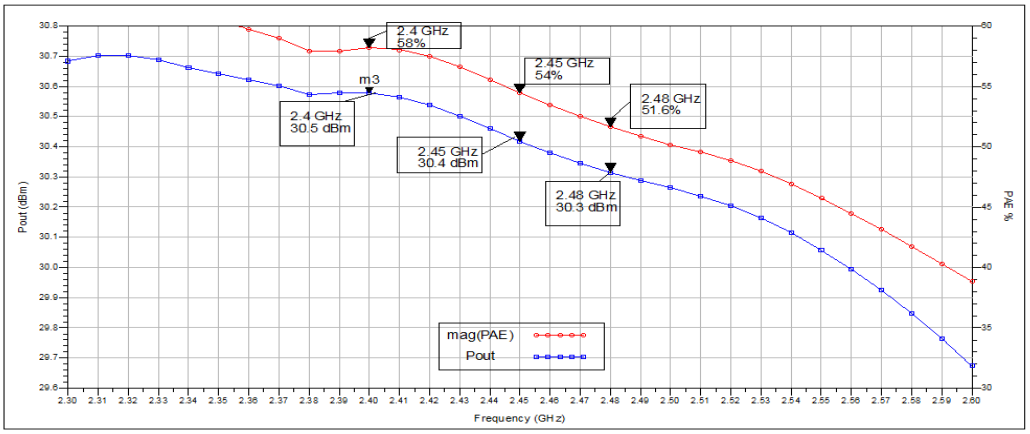


Figure (13): The performance of the PA based on PSCT as a function of frequency.

EM-Simulation of the Proposed Transformer

The power combining transformer PSCT is implemented with four primary inductors i.e. four power amplifier stages. The PSCT is composed of a series combining

of two PCTs that have two primary inductors interwoven to the secondary inductor. Thus, the transformer exhibits a series-combining of two parallel-combining parts (i.e., N_P = 2, N_S = 2) with the total combining inputs of M = 4 .The turn ratio of the PCT is (N_P×1: n) is used fixed to ensure that (N_S =N_P).The transformer was implemented using two thick metals (4μm-thick aluminum and 3μm-thick copper) that are connected through whole via trace as shown in Figure (14). The width of the inductor metal traces (30 μm) was chosen. The EM simulation shows that each primary inductor and the secondary inductor have the self inductance of 0.8 nH and 3.8 nH with quality factor the of 11.6 and 9 at 2.45 GHz, respectively, the size of the PSCT layout is 1.36×0.52 mm^2. The quality factor (Q) can be expressed by the ratio between the imaginary and real part of the input impedance [14]:

$$Q_1 = \frac{imag(Z_{11})}{real(Z_{11})} = \frac{imag\left(1/Y_{11}\right)}{real\left(1/Y_{11}\right)} \quad ...(19)$$

$$Q_2 = \frac{imag(Z_{22})}{real(Z_{22})} = \frac{imag\left(1/Y_{22}\right)}{real\left(1/Y_{22}\right)} \quad ...(20)$$

The inductance can be extracted from the input resistance:

$$L_1 = \frac{imag\,(Z_{11})}{\omega} = \frac{imag\left(1/Y_{11}\right)}{\omega} \quad ...(21)$$

$$L_2 = \frac{imag\,(Z_{22})}{\omega} = \frac{imag\left(1/Y_{22}\right)}{\omega} \quad ...(22)$$

The EM simulation results are shown in Figure (15) and Figure (16), for the primary and secondary inductors, respectively. The efficiency of the PSCT measured using Equation (6) at 2.45 GHz is 78% as shown in Figure (17). The minimum insertion loss (*ILmin*) of the transformer is shown in Figure (18), calculated by the following equation [15] :

$$IL_{min}\ (dB) = 10\log_{10}\left[1 + \frac{2}{(K^2 Q_p Q_s)} + 2\sqrt{\frac{1}{(K^2 Q_p Q_s)}\left(1 + \frac{1}{(K^2 Q_p Q_s)}\right)}\right] \quad ...(23)$$

Figure (19) shows the EM simulation of the current density of the transformer, a good distribution of the current is clear, which is a direct thermal effect of the coil. The simplified schematic of the proposed PA based on PSCT is shown in Figure (20).

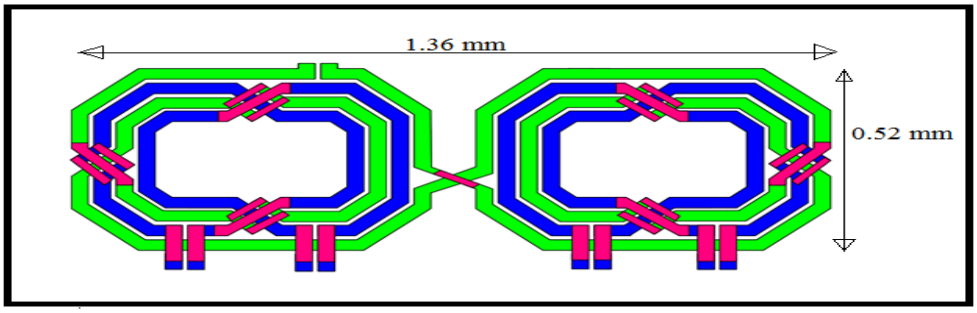
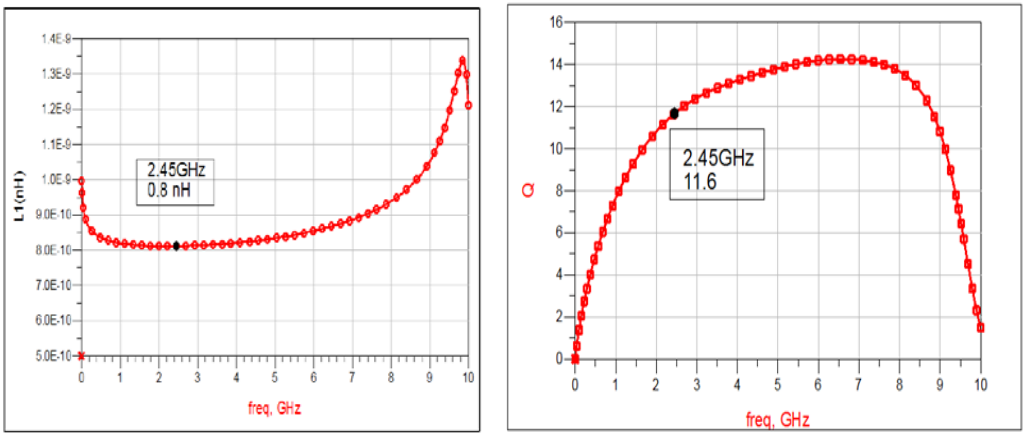
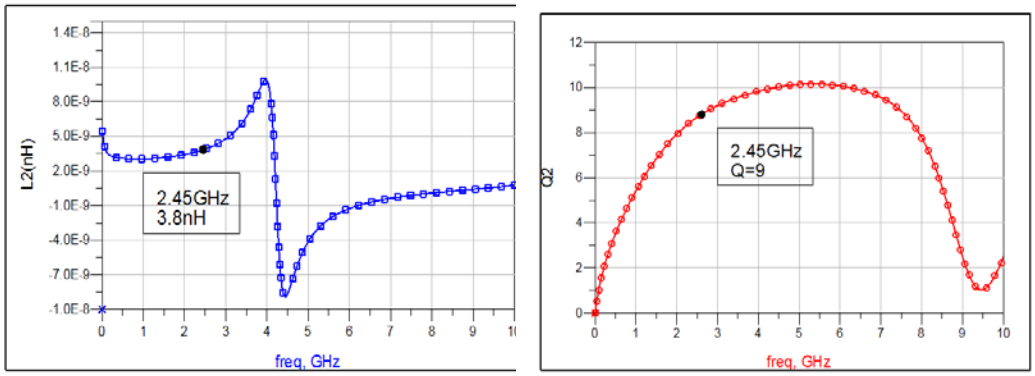


Figure (14): The Conceptual diagram of the transformer



(a) **(b)**

Figure (15): Simulation results for the primary inductor. (a) Self inductance.



(a) **(b)**

Figure (16): Simulation results for the secondary inductor. (a) Self inductance. (b) Quality factor.

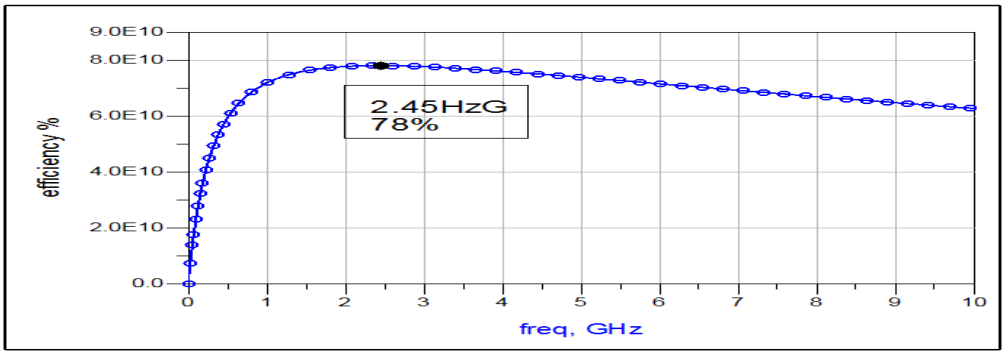


Figure (17): Calculated efficiency of the PSCT.

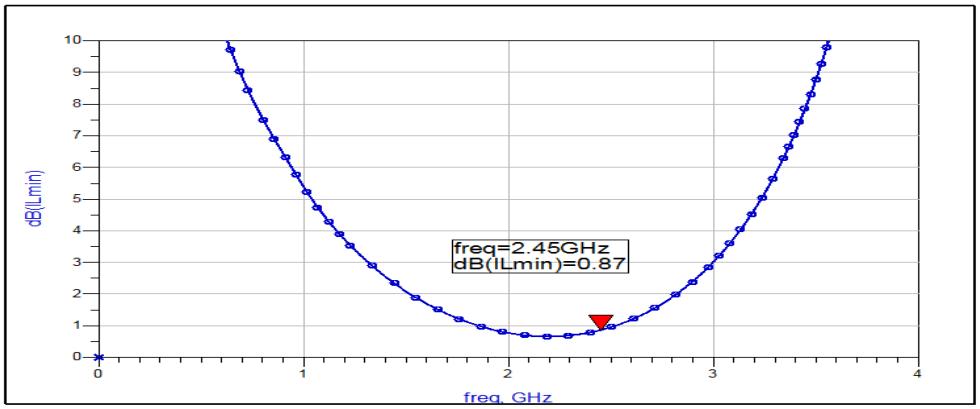


Figure (18): Simulated insertion loss of the transformer.

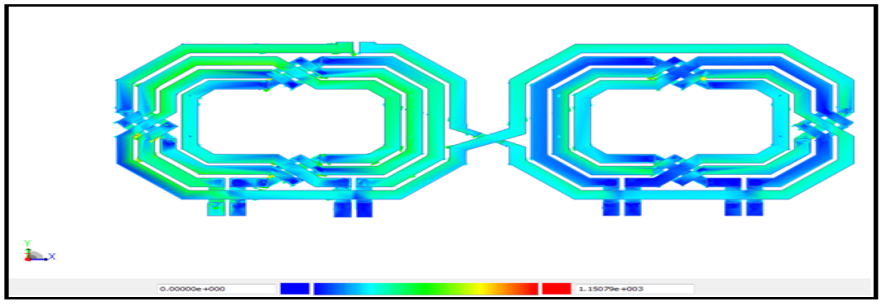


Figure (19): Current density simulation of the transformer.

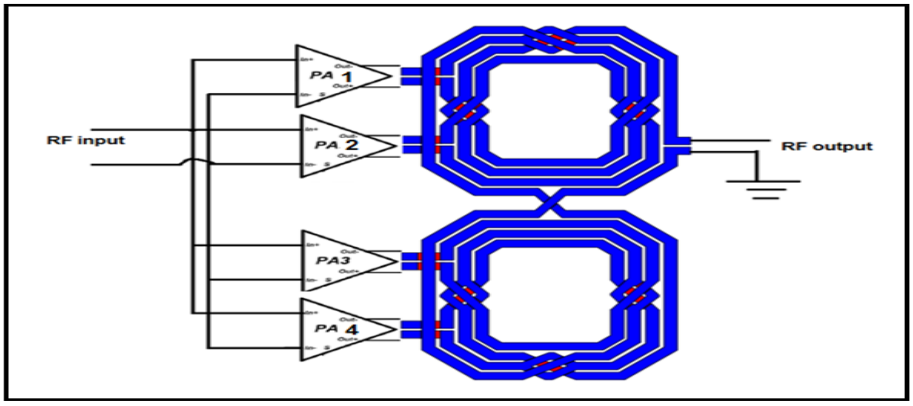


Figure (20):A Simplifies schematic diagram of the designed PA.

Conclusion

A hybrid-type (parallel-series) power-combining transformer was designed to implement a fully-integrated watt level CMOS PA. The designed PA incorporates four stages differential PA based on PSCT. Linear PA class_AB designed for WLAN applications, it delivers an output power of 30 dBm with PAE of 40% using 2.5 V supply voltage. Nonlinear PA class_E designed to deliver an output power of 30 dBm with PAE of 54% using 1.6 V supply voltage.

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